USER GUIDE



Common Management Interface Kit

CMIS GUI User Guide – CMIS Rev3.0/4.0 Compliant Revision 0.2 October 2021

QSFP-DD Host – QSFP Host – DSFP Host – SFP-DD Host – OSFP Host

Innovation for the next generation



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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the General Safety Summary in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Only use the power cord specified for this product and certified for the country of use.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal that exceeds the maximum rating of that terminal.

Do Not Operate Without Covers.

Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate with Suspected Failures.

If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions. Do Not Operate in an Explosive Atmosphere. Keep Product Surfaces Clean and Dry

Caution statements identify conditions or practices that could result in damage to this product or other property.



Table of Contents

		• • • • • • • • • • • • • • • • • • • •
1.	Installation & Running	•••••
2.	CMIS Version	
3.	Communication	
4.	GUI Sections	
	4.1 Monitor	
	4.2 Interrupt Masks	
	4.3 Controls	
	4.4 Low Speed Signals	
	4.4.1 QDD Family	
	4.4.2 OSFP Family	
	4.4.3 DSFP Family	
	4.4.4 QSFP Family	
	4.4.5 SFP-DD Family	
	4.5 Identification	
	4.6 Options Available	
	4.7 Load/Save MSA	
	4.8 Load/Save Page 10/11h	
	4.9 I2C R/W	
	4.10 QDD MXP	
	4.11 I2C R/W Advanced	
	4.12 Command Data Block (CDB) Message Communication	
	4.12.1 CDB Commands	
	CMD 0000h Query Status	
	CMD 0001h Enter Password	
	 CMD 0002h Change Password CMD 0002h Enable (Display Decement Protection) 	
	CMD 0003h Enable/Disable Password Protection	
	CMD 0004h General Abort	
	 CIVID 0380II LOOPDACKS 4 12 2 CDP Easture and Canabilities Commands 	
	4.12.2 CDB Feuture una capabilities commands	
	CMD 0042h Performance Monitoring	
	CMD 0042h Performance Monitoring CMD 0043h Bert and diagnostics	
	CMD 0041h Bead EW Eastures	
	4 12 3 CDB Firmware Download Commands	
	CMD 0101h 0103h 0107h Program I PI	
	 CMD 0101h, 0103h, 0107h Program EPI CMD 0101h 0104h 0107h Program EPI 	
	 CMD 0101h, 0105h, 0107h Read Image I PI 	
	 CMD 0101h, 0106h, 0107h Read Image EPI CMD 0101h, 0106h, 0107h Read Image EPI 	
	 CMD 0102h Abort FW download 	
	 CMD 0109h Run image 	
	 CMD 010Ah Commit image 	
	 CMD 0108h Copy image A to B/B to A 	
	 CMD 0100h Get FW Info 	
	4.12.4 CDB Performance/Data Monitoring Commands	
	 CMD 0200h PM Controls 	
	CMD 0201h PM Feature Information	
	 CMD 0280h Data Monitoring and Recording Controls 	
	CMD 0281h Data monitoring and recording	
	CMD 0290h Temperature Histogram	
	CMD 0210h, 0211h Get Module PM LPL/EPL	
	 CMD 0212h, 0213h Get PM Host Side LPL/EPL 	
	CMD 0214h, 0214h Get PM Media Side LPL/EPL	



Revision Control

Revision number	Description	Release Date
0.1	 Initial version 	4/20/2020
0.22	Added CDB FeatureFormat updates	10/12/2021

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List of Acronyms

Acronym	Definition
CMIS	Common Management Interface Kit
CDB	Command Data Block
BW	Bandwidth
BERT	Bit Error Rate Tester
Conf	Configuration
DUT	Device Under Test
FEC	Forward Error Correction
FW	Firmware
GBd	Gigabaud
Gbps	Gigabits per Second
GUI	Graphical User Interface
HW	Hardware
SI	Signal Integrity
Sim	Simulation
SW	Software



Introduction

The ML-CMIS GUI is a common software interface that allows to communicate with, operate and control various MCBs boards. It allows to utilize a common software across a variety of form factors. The ML-CMIS GUI communicate with the host board through USB connection. The communication is established after installing the proper driver of the target host.

The ML-CMIS GUI allows to communicate on multiple hosts simultaneously, by assigning different USB instance to each host.

The various hosts operating with the ML-CMIS GUI are listed below:

- QDD800 host
- QDD host
- OSFP host
- QSFP host
- SFP-DD host
- DSFP host



GUI Introduction

1. Installation & Running

The GUI installation file is available on the website. User could download it under the target product page.

To install the GUI, simply double-click on the installer file, and follow the instructions. For Windows version newer than Windows 7 the GUI must be run as administrator. A message box will pop-up for confirmation.



Figure 1: Pop-up message

After the GUI runs properly, a window will open as shown below.

m Commo	n Mana	gement Inte	erface Kit													- 0	×
									Com	munication							
multi	Lar	1 e _{sal} _		~		A			Sele	ect Device Type	QDD Ho	st v US	B instance:	paitor	About II	Module Found Module Not Fou	ind
Cor	nm	on N	/lana	ger	nent	t Inte	erface	e Kit		initiatize	Ken	esii	Pause ma	JIIICOI	About o	USB Connected	
			CMI	Vers	ion: 3	0											
			SWI	ten to (LMIS 4.0												
Monitor																	
	Mode	In Manitor					Internuol	t Elbar									
	mou						Alamas	c i tags			Manaia						
	Ch	RX LOS T			L TX Fault	t State Cng	Alarms	RY Power	TY Rias	TY Power	warnin	RX Power	TY Bias	TX Power		State Changed	
	1						Ch	High Low	High Low	High Low	Ch	High Low	High Low	High Low		Juice changed	
	2						1				1						
	3						2				2						
	4						3				3						
	5						4				4						
	0						5				5						
	8						6				6						
	ľ						7				7						
	Char	and a Manala					8				8						
	Criar	inets monito	or ⊖ dBm	۲	mW			High Lov	~	High Low		High Lo	w	High Low			
	Ch	RX Po	wer T)	Bias	TX Pov	ver	Temp		AUX 1		Temp		AUX 1				
	1						VCC 3	.3 0 0	AUX 2		VCC 3	.3 (AUX 2				
	2					_	Vendor	Def 🔿 🔿	AUX 3		Vendor	Def	AUX 3				
	3																
							Module /	Nonitor			_		MCB VCC N	lonitor	MCE	3 Current Monitor	
							Temp		A	UX1(TEC curre	nt)		VCC:		Cur	rrent VCC:	
							Supply	3.3V	A	UX2(TEC curre	nt)		VCC1:		Cur	rrent VCCTX:	
	0								A	UX3(Laser Tem	p)		(Only for	QDD-MXP)	Cur	rent VCCRX:	
	7												VCCTX:				J
	8												VCCRX:				
																	1

Figure 2: GUI Window

7



2. CMIS Version

The GUI covers the CMIS 3.0 and CMIS 4.0. The user must choose the CMIS version first.



Figure 3: CMIS Version Selection

By clicking on the button shown above, the user can switch between CMIS 3.0 and CMIS 4.0. Depending on the CMIS Version chosen by the user, the list of devices will change. Below is a summary of supported hosts based on CMIS version.

- CMIS Version 3.0
 - o QDD Host
 - OSFP Hosts (ML4064-TR is under the OSFP family)
- CMIS Version 4.0
 - QDD Hosts (ML4062-TR is under the QDD family)
 - OSFP Hosts (ML4064-TR is under the OSFP family)
 - o QSFP Host
 - o SFP-DD Host
 - o DSFP Host

3. Communication

The communication between the GUI and the host is established from the Communication window. Under this window, the user can select the Device Type and the USB instance.

The connection is established by clicking the Initialize button. This button is the application main entry point. Once a USB connection is established, the Host checks if a Module is inserted, and accordingly illuminates the corresponding (Module Found or Module Not Found) LED. If a Module is inserted, the initialization process proceeds with checking the related Hardware pins to ensure that the module is selected and ready to communicate with host.

Also, the following buttons are available in the Communication window.

Refresh button: Checks for connection status, refresh Hardware Readings and updates GUI. Pause Monitor button: Pause/Resume monitoring.

About Us button: Shows software information (name, version) and company information.

Initialize Refresh Pause Monitor About Us USB Connected	Initialize Refresh Pause Monitor About Us USB Connect
USB Error	O OSB EITO

Figure 2: Communication Tab



4. GUI Sections

The ML-CMIS GUI contains the following tabs:

- Monitor
- Interrupt Masks
- Controls
- Low Speed Signals
- Identification
- Options Available
- Load/Save MSA
- Load/Save Page 10/11h
- I2C R/W
- I2C R/W Advanced
- DVT
- QDD-MXP (only for QSFP-DD Host)

All these tabs are common for all hosts. The subsequent sections will cover each tab separately. Any difference between various hosts in a specific tab will be mentioned explicitly.

4.1 Monitor

The Monitor tab shows the digital diagnostic monitoring flags status.

All alarms and warnings are expressed with LEDs as shown in Figure 5, when a flag is asserted, the corresponding LED turns ON (becomes red), when not asserted the LED remains transparent.

Also, the Monitor tab shows measurements of various monitoring values (voltage, current and temperature) and are displayed continuously.

Two main measurements windows are available:

- 1 Module Monitor
- 2 MCB Monitor

Note that the measured quantities differ from MCB to another depending on the implementation.

Mod	ule Monitor					Interrupt	Flags								
Ch	RX LOS TX	OS RX LC	L TX LOL	TX Fault	State Cng	Alarms				Warning	şs				
1							RX Power	TX Bias	TX Power		RX Power	TX Bias	TX Power	0	State Change
2						Ch	High Low	High Low	High Low	Ch	High Low	High Low	High Low		
3						1				1					
						2				2					
4						3				3					
5						4				4					
6						5				5					
7						6				6					
8						7				7					
						8				8					
Char	nnels Monito				_										
	C) dBm	۲	mW			High Lov	w +	high Low		High Lo	w	High Low		
Ch	RX Pow	er T)	Bias	TX Pow	er	Temp		AUX 1		Temp		AUX			
1						VCC 3.	.3 O C	AUX 2		VCC 3	.3 () ()	AUX 2			
2						Vendor	Def 🔿 🔿	AUX 3		Vendor	Def 🔿 🤇	AUX 3			
3						Module A	Ionitor				1	MCB VCC /	Nonitor	MCB Cur	rent Monitor
4						Temp		AU	IX1(TEC curre	nt)		VCC:		Current	VCC:
5						Supply	3.3V	AU	X2(TEC curre	nt)		VCC1.		Current	VCCTV.
6								41	IX3/I aser Tem	-		(Only for	ODD-MXP)	current	VCC1A:
7						_		AU	ASTERIO ICIII	P)		VCCTV-	(00 mod)	Current	VCCRX:
												VCCIA.			

Figure 5: Monitor Tab



The following table shows the MSA memory mapping for the monitoring tab objects.

Byte	Bit		Name	Description	Туре
14	7-	0	Module Monitor 1:	Internally measured temperature: signed 2's	RO
		-	Temperature MSB	complement in 1/256 degree Celsius increments	Opt.
				NOTE: Temp can be below 0.	
15	7	0	Madula Manitar 1		
15	/-	0	Tomporatural LSB		
16	7	0	Medule Meniter 2: Cupply	Internally macquired 2.2 yelt input cumply yeltages in	DO
10	/-	0	2.2 volt MSP	100 uV increments	Opt
17	7	0	Madula Manitar 2: Supply	100 µV increments	Opt.
17	/-	0	2.2 volt LCP		
10	7	0	Modulo Monitor 2: Aux 1	TEC Current or Decenved monitor	PO.
10	/-	0	MODULE MOTILOI 5. AUX 1	TEC Current: signed 2's complement in 1/32767%	Opt
10	7	0	Modulo Monitor 2: Aux 1	incroments of maximum TEC current	Opt.
19	/-	0		± 32767 is may TEC current (100%) $=$ May Heating	
			LSD	-32767 is min TEC current (100%) – Max fielding	
20	7-	0	Module Monitor 4: Aux 2	TEC Current or Laser Temperature monitor TEC Current:	RO
20	· '	0	MSB	signed 2's complement in 1/32767% increments of	Opt
21	7-	0	Module Monitor 4: Aux 2	maximum TEC current	Opt.
21	· '	0	I SB	+32767 is max TEC current (100%) – Max Heating	
			250	-32767 is min TEC current (100%) – Max Cooling	
				Laser Temperature: signed 2's complement in 1/256	
				degree Celsius increments	
				See Page 01h Byte 145 Table Table 8-30	
22	7-	0	Module Monitor 5: Aux 3	Laser Temperature or additional supply voltage monitor	RO
		-	MSB	Laser Temperature: signed 2's complement in 1/256	Opt.
				degree Celsius increments	
23	/-	0	Module Monitor 5: Aux 3	Additional supply voltage monitor: in 100 µV increments	
			LSB	See Page 01h Byte 145 Table Table 8-30	
24	7-	0	Module Monitor 6: Custom	Custom monitor	RO
21	· '	0	MSB		Opt
25	7-	0	Module Monitor 6: Custom	_	opu.
25	1	0	I SB		
8	7		DB block 2 complete	Latched flag to indicate completion of the CDB command fo	r PO Opt
Ŭ	1		DD block 2 complete	CDB block 2 Clear on Read (See Page 01b, Byte 163 bit 7)	
	6	1-0	DB block 1 complete	Latched flag to indicate completion of the CDB command for	r RO Opt
	0	1-0	DD block I complete	CDB block 1 Clear on Read (See Page 01b, Byte 163 bit 6)	
	5-3	Rec	erved		ROD
	2	Dat	a Path firmware fault	Some modules may contain an auxiliary device for	RQD RQ Ont
	2	Dat		processing the transmitted and received signals (e.g. a	KO Opt.
				DSP) The Data Path Firmware Fault flag becomes set when	
				an integrity check of the firmware for this auxiliary device	
				finds an error	
	1	Mo	lule firmware fault	The Module Firmware Fault flag becomes set when an	RO
	-	1100		integrity check of the module firmware finds an error. There	Opt
				are several possible causes of the error such as program	
				memory becoming corrupted and incomplete firmware	
				loading.	
	0	I-M	odule state changed flag	Latched Indication of change of Module state (see Table	RO ROD
	0		budie state changed hag	8-5) Clear on Read	NO NQU
0	7	L-V	cc3 3v Low Warping	Latched low 3.3 volts supply voltage warping flag. Clear on	PO Opt
9	/	L-V		Pead	KO Opt.
	6	1.1	cc3 3v High Warning	Latched high 3.3 volts supply voltage warping flag. Clear on	
	0	L-V		Read	
	5	1-1/	cc3 3v Low Alarm	Latched low 3.3 volts supply voltage alarm flag. Clear on	-
	5	L-V		Pead	
	1	1.1	cc3 3v High Alarm	Latched high 3.3 volte cupply voltage plarm flag. Clear an	-
	4	L-V		Latened myn 5.5 voits supply voitage alarm nag. Clear on Dead	
	2	I	amp Low Warping	Latched low temperature warning flag. Clear on Poad	-
	<u> </u>			Latched high temperature warning flag. Clear on Read	-
	4			Latched low temperature elarm flar. Clear on Kead	-
	1			Latched high temperature alarm flag. Clear on Kead	-
	U	L-1	emp Hign Alarm	Latched high temperature alarm flag. Clear on Read	

10	7	L-Aux 2 Low Warning	Latched low warning for Aux 2 monitor. Clear on Read
	6	L Aux 2 High Warping	Latched high warning for Aux 2 monitor. Clear on Read
	5		Latched low alarm for Aux 2 monitor. Clear on Read
	5	L-Aux 2 Low Alarm	Latched high alarm for Aux 2 monitor. Clear on Read
	7	L-Aux 2 High Aldrin	Latched low warring for Aux 1 monitor. Clear on Read
	2	L-Aux 1 Low Warning	Latched high warning for Aux 1 monitor. Clear on Read
	- 2		Latched low alarm for Aux 1 monitor. Clear on Read
	1	L-Aux 1 Llow Alarm	Latched high alarm for Aux 1 monitor. Clear on Read
		L-Aux I High Alarm	Latched high alarm for Aux 1 monitor. Clear on Read
11	/	L-Vendor Defined Low Warning	Read
	6	L-Vendor Defined High Warning	Latched high warning for Vendor Defined Monitor. Clear on Read
	5	L-Vendor Defined Low Alarm	Latched low alarm for Vendor Defined Monitor. Clear on Read
	4	L-Vendor Defined High Alarm	Latched high alarm for Vendor Defined Monitor. Clear on Read
	3	L-Aux 3 Low Warning	Latched low warning for Aux 3 monitor. Clear on Read
	2	L-Aux 3 High Warning	Latched high warning for Aux 3 monitor. Clear on Read
	1	L-Aux 3 Low Alarm	Latched low alarm for Aux 3 monitor. Clear on Read
	0	L-Aux 3 High Alarm	Latched high alarm for Aux 3 monitor. Clear on Read
12	7-0	Reserved	
13	7-0	Custom	
Byte	Bit	Name	Description
134	7	L-Data Path State Changed flag, host lane 8	Latched Data Path State Changed flag for host lane 8
	6	L-Data Path State changed flag, host lane 7	Latched Data Path State Changed flag for host lane 7
	5	L-Data Path State Changed flag, host lane 6	Latched Data Path State Changed flag for host lane 6
	4	L-Data Path State Changed flag, host lane 5	Latched Data Path State Changed flag for host lane 5
	3	L-Data Path State Changed flag, host lane 4	Latched Data Path State Changed flag for host lane 4
	2	L-Data Path State Changed flag, host lane 3	Latched Data Path State Changed flag for host lane 3
	1	L-Data Path State Changed flag, host lane 2	Latched Data Path State Changed flag for host lane 2
	0	L-Data Path State Changed flag, host lane 1	Latched Data Path State Changed flag for host lane 1
135	7	L-Tx8 Fault flag	Latched Tx Fault flag, media lane 8
	6	L-Tx7 Fault flag	Latched Tx Fault flag, media lane 7
	5	L-Tx6 Fault flag	Latched Tx Fault flag, media lane 6
	4	L-Tx5 Fault flag	Latched Tx Fault flag, media lane 5
	3	L-Tx4 Fault flag	Latched Tx Fault flag, media lane 4
	2	L-Tx3 Fault flag	Latched Tx Fault flag, media lane 3
	1	L-Tx2 Fault flag	Latched Tx Fault flag, media lane 2
	0	L-Tx1 Fault flag	Latched Tx Fault flag, media lane 1
136	7	L-Tx8 LOS flag	Latched Tx LOS flag, lane 8
	6	L-Tx7 LOS flag	Latched Tx LOS flag, Jane 7
	5	L-Tx6 LOS flag	Latched Tx LOS flag, Jane 6
	4	L-Tx5 LOS flag	Latched Tx LOS flag, Jane 5
	3	L-Tx4 LOS flag	Latched Tx LOS flag, Jane 4
	2	L-Tx3 LOS flag	Latched Tx LOS flag, Jane 3
	1	I-Tx2 LOS flag	Latched Tx LOS flag, Jane 2
	0		Latched Tx LOS flag, Jane 1
	v		Eached TA EOU hdy, idne 1
137	7		Latched Ty CDR LOL flag Jane & Clear on Pead

ult		ane		
	6	L-Tx7 CDR LOL flag	Latched Ty CDR LOL flag, Jane 7, Clear on Read	0
			Latched Tx CDR LOL flag, Jane 6. Clear on Read	łٽ
	J 		Latched TX CDR LOL flag, Jane C. Clear on Read	-
	4	L-TX5 CDR LOL flag	Latched TX CDR LOL flag, lane 5. Clear on Read	_
	3	L-1x4 CDR LOL flag	Latched Tx CDR LOL flag, lane 4. Clear on Read	
	2	L-Tx3 CDR LOL flag	Latched Tx CDR LOL flag, lane 3. Clear on Read	
	1	L-Tx2 CDR LOL flag	Latched Tx CDR LOL flag, lane 2. Clear on Read	
	0	L-Tx1 CDR LOL flag	Latched Tx CDR LOL flag, lane 1. Clear on Read	
138	7	L-Tx8 Adaptive Input Eq Fault Lane 8 flag	Latched Tx Adaptive Input Eq. Fault Lane 8. Clear on Read	R O
	6	L-Tx7 Adaptive Input Eq Fault Lane 7 flag	Latched Tx Adaptive Input Eq. Fault Lane 7. Clear on Read	
	5	L-Tx6 Adaptive Input Eq Fault Lane 6 flag	Latched Tx Adaptive Input Eq. Fault Lane 6. Clear on Read	
	4	L-Tx5 Adaptive Input Eq Fault Lane 5 flag	Latched Tx Adaptive Input Eq. Fault Lane 5. Clear on Read	
	3	L-Tx4 Adaptive Input Eq Fault Lane 4 flag	Latched Tx Adaptive Input Eq. Fault Lane 4. Clear on Read	
	2	L-Tx3 Adaptive Input Eq Fault Lane 3 flag	Latched Tx Adaptive Input Eq. Fault Lane 3. Clear on Read	
	1	L-Tx2 Adaptive Input Eq Fault Lane 2 flag	Latched Tx Adaptive Input Eq. Fault Lane 2. Clear on Read	
	0	L-TXI Adaptive Input Eq Fault Lane 1 flag	Latched 1x Adaptive Input Eq. Fault Lane 1. Clear on Read	
139	7	L-Tx8 Power High alarm	Tx output power High Alarm, media lane 8. Clear on Read	_ R
	6	L-Tx7 Power High alarm	Tx output power High Alarm, media lane 7. Clear on Read	_ 0
	5	L-Tx6 Power High alarm	Tx output power High Alarm, media lane 6. Clear on Read	-
	4	L-1x5 Power High alarm	Ix output power High Alarm, media lane 5. Clear on Read	-
	3	L-1x4 Power High alarm	Tx output power High Alarm, media lane 4. Clear on Read	-
		L-1x3 Power High alarm	Tx output power High Alarm, media lane 3. Clear on Read	-
	1	L-IX2 Power High alarm	Tx output power High Alarm, media lane 2. Clear on Read	-
140	7	L-TX1 Power High alarm	Tx output power High Alarm, media lane 1. Clear on Read	
140	6	L-Tx7 Power Low alarm	Tx output power Low alarm, media lane 5. Clear on Read	
	5	L-Tx6 Power Low alarm	Tx output power Low alarm, media lane 7: Clear on Read	1~
	4	L-Tx5 Power Low alarm	Tx output power Low alarm, media lane 5. Clear on Read	-
	3	L-Tx4 Power Low alarm	Tx output power Low alarm, media lane 5. Clear on Read	-
	2	L-Tx3 Power Low alarm	Tx output power Low alarm, media lane 3. Clear on Read	-
	1	L-Tx2 Power Low alarm	Tx output power Low alarm, media lane 2. Clear on Read	-
	0	L-Tx1 Power Low alarm	Tx output power Low alarm, media lane 1. Clear on Read	-
141	7	L-Tx8 Power High warning	Tx output power High warning, media lane 8. Clear on Read	R
171	6	L-Tx7 Power High warning	Tx output power High warning, media lane 7. Clear on Read	
	5	L-Tx6 Power High warning	Tx output power High warning, media lane 6. Clear on Read	╡҇
	4	L-Tx5 Power High warning	Tx output power High warning, media lane 5. Clear on Read	1
	3	L-Tx4 Power High warning	Tx output power High warning, media lane 4. Clear on Read	1
	2	L-Tx3 Power High warning	Tx output power High warning, media lane 3. Clear on Read	
	1	L-Tx2 Power High warning	Tx output power High warning, media lane 2. Clear on Reads	ettin
	0	L-Tx1 Power High warning	Tx output power High warning, media lane 1. Clear on Read	
142	7	L-Tx8 Power Low warning	Tx output power Low warning, media lane 8. Clear on Read	R
- 12	6	L-Tx7 Power Low warning	Tx output power Low warning, media lane 7. Clear on Read	
	5	L-Tx6 Power Low warning	Tx output power Low warning, media lane 6. Clear on Read	1
	-		To establish a super la supere	-

ult		ane		
		••		
Ļ	3	L-Tx4 Power Low warning	Tx output power Low warning, media lane 4. Clear on Read	
ŀ	2	L-Tx3 Power Low warning	Tx output power Low warning, media lane 3. Clear on Read	
ŀ	1	L-Tx2 Power Low warning	Tx output power Low warning, media lane 2. Clear on Read	
	0	L-Tx1 Power Low warning	Tx output power Low warning, media lane 1. Clear on Read	
143		L-Tx8 Bias High Alarm	Tx Bias High Alarm, media lane 8. Clear on Read	
F	6	L-Tx7 Bias High Alarm	Tx Bias High Alarm, media lane 7. Clear on Read	
ŀ	5	L-Tx6 Bias High Alarm	Tx Bias High Alarm, media lane 6. Clear on Read	
ŀ	4	L-Tx5 Bias High Alarm	Tx Bias High Alarm, media lane 5. Clear on Read	
ŀ	3	L-Tx4 Bias High Alarm	Tx Bias High Alarm, media lane 4. Clear on Read	
ŀ	2	L-Tx3 Blas High Alarm	Tx Bias High Alarm, media lane 3. Clear on Read	
ŀ	1	L-Tx2 Bias High Alarm	Ix Bias High Alarm, media lane 2. Clear on Read	
	0	L-Tx1 Bias High Alarm	Ix Bias High Alarm, media lane 1. Clear on Read	
144	/	L-1x8 Blas Low alarm	Tx Bias Low alarm, media lane 8. Clear on Read	
ŀ	6	L-TX/ Blas Low alarm	Tx Blas Low alarm, media lane 7. Clear on Read	
ŀ	5	L-Tx6 Blas Low alarm	Tx Bias Low alarm, media lane 6. Clear on Read	
ŀ	4	L-Tx5 Blas Low alarm	TX Blas Low alarm, media lane 5. Clear on Read	
ŀ	3	L-TX4 Blas Low alarm	TX Blas Low alarm, media lane 4. Clear on Read	
ŀ		L-Tx3 Blas Low alarm	Tx Blas Low alarm, media lane 3. Clear on Read	
ŀ	1	L-Tx2 Blas Low alarm	Tx Blas Low alarm, media lane 2. Clear on Read	
145		L-TXI Blas Low alarm	Tx Bias Low alarm, media lane 1. Clear on Read	
145		L-Tx8 Blas High warning	Tx Bias High warning, media lane 8. Clear on Read	
ŀ	<u> </u>	L-TX/ Blas High warning	Tx Bias High warning, media lane 7. Clear on Read	
ŀ	5	L-Tx6 Blas High warning	Tx Bias High warning, media lane 6. Clear on Read	
ŀ	4	L-Tx5 Blas High warning	Tx Bias High warning, media lane 5. Clear on Read	
ŀ	<u> </u>	L-Tx4 Bias High warning	Tx Bias High warning, media lane 4. Clear on Read	
ŀ		L-Tx3 Bias High warning	Tx Bias High warning, media lane 3. Clear on Read	
ŀ	- 1	L-TX2 Dids High warning	Tx Dias High warning, media Jane 1. Clear on Read	
146	7		Tx Bias Low warning, media Jane 8, Clear on Read	
140	6	L-Txo Bias Low warning	Tx Dias Low warning, media Jane 7. Clear on Read	
ŀ	5	L-TX/ Bias Low warning	Tx Bias Low warning, media Jane 6. Clear on Read	
ŀ		L Type Bias Low warning	Tx Bias Low warning, media Jane E. Clear on Read	
ŀ	2	L-Tx3 Blas Low warning	Tx Bias Low warning, media Jane 4. Clear on Read	
ŀ	2	L-Tx3 Bias Low warning	Tx Bias Low warning, media lane 3. Clear on Read	
ŀ	1	L-Tx2 Bias Low warning	Tx Bias Low warning, media lane 3. Clear on Read	
ŀ	0	L-Tx1 Bias Low warning	Tx Bias Low warning, media lane 2. Clear on Read	
147	7		Latched By LOC flag, media lane 1. Clear on Read	Т
14/	6		Latched Ry LOS flag, media Jane 7. Clear on Read	$\left \right $
ŀ			Latched Ry LOS flag, media Jane 6. Clear on Read	
ŀ	<u> </u>		Latched Ry LOS flag, media Jane 5. Clear on Read	
ŀ	2		Latched Ry LOS flag, media Jane 4. Clear on Read	
ŀ	2		Latched Ry LOS flag, media lane 3. Clear on Pead	
ŀ	1		Latched Ry LOS flag, media lang 2. Clear on Pead	
ŀ	1		Latched Ry LOS flag, media lang 1. Clear on Pead	
148	7		Latched Ry CDR LOL flag, media lane 8. Clear on Pead	+
110	6		Latched Ry CDR LOL flag, media lane 7. Clear on Read	
ŀ	5		Latched Ry CDR LOL flag, media lane 6. Clear on Read	
ŀ	4		Latched Ry CDR LOL flag, media lane 5. Clear on Read	
ŀ	1			1

multiLane	
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	2	L-Rx3 CDR LOL		Latched Rx CDR LOL flag, media lane 3. Clear on Read	
	1	L-Rx2 CDR LOL		Latched Rx CDR LOL flag, media lane 2. Clear on Read	
	0	L-Rx1 CDR LOL		Latched Rx CDR LOL flag, media lane 1. Clear on Read	
149	7	L-Rx8 Power High ala	rm	Rx input power High alarm, media lane 8. Clear on Read	RO
	6	L-Rx7 Power High ala	rm	Rx input power High alarm, media lane 7. Clear on Read	Opt.
	5	I-Rx6 Power High ala	rm	Rx input power High alarm, media lane 6. Clear on Read	
	4	L-Rx5 Power High alar	rm	Rx input power High alarm, media lane 5. Clear on Read	
	3	I-Rx4 Power High ala	rm	Rx input power High alarm, media lane 4 Clear on Read	
	2	L-Rx3 Power High ala	rm	Rx input power High alarm, media lane 3. Clear on Read	
	1	L-Rx2 Power High ala	rm	Rx input power High alarm, media lane 2. Clear on Read	
	0	L-Rx1 Power High ala	rm	Rx input power High alarm, media lane 1. Clear on Read	
150	7	L-Rx8 Power Low alar	m	Ry input power Low alarm, media lane 8. Clear on Read	RO
150	6	L-Ry7 Power Low alar	m	Ry input power Low alarm, media lane 7. Clear on Read	Ont
	5	L-Rx6 Power Low alar	m	Py input power Low alarm, media lane 6. Clear on Read	opt.
	1	L PyE Power Low alar	m	Py input power Low alarm, media lane 6. Clear on Read	
	2	L-Rx4 Power Low alar	m	Py input power Low alarm, media lane 5. Clear on Read	
	2	L By2 Dower Low alar		Rx input power Low alarm, media lane 4. Clear on Read	
	1	L-RX3 FOWEI LOW alar		Rx input power Low alarm, media lane 3. Clear on Read	
	1	L-RX2 POWer Low alar	···	Rx input power Low alarm, media lane 2. Clear on Read	
454		L-RX1 Power Low alar	m 	Rx input power Low alarm, media lane 1. Clear on Read	D O
151	1	L-RX8 Power High wai	rning	RX input power High warning, media lane 8. Clear on Read	RU
	6	L-RX/ Power High wai	rning	RX input power High warning, media lane 7. Clear on Read	Opt.
	5	L-Rx6 Power High Wal	rning	RX input power High warning, media lane 6. Clear on Read	
	4	L-Rx5 Power High wai	rning	Rx input power High warning, media lane 5. Clear on Read	
	3	L-Rx4 Power High wai	rning	Rx input power High warning, media lane 4. Clear on Read	
	2	L-Rx3 Power High wai	rning	Rx input power High warning, media lane 3. Clear on Read	
	1	L-Rx2 Power High wai	rning	Rx input power High warning, media lane 2. Clear on Read	
1.50	0	L-Rx1 Power High warning		Rx input power High warning, media lane 1. Clear on Read	
152	/	L-Rx8 Power Low war	ning	Rx input power Low warning, media lane 8. Clear on Read	RO
	6	L-Rx/ Power Low war	ning	Rx input power Low warning, media lane /. Clear on Read	Opt.
	5	L-Rx6 Power Low war	ning	Rx input power Low warning, media lane 6. Clear on Read	
	4	L-Rx5 Power Low war	ning	Rx input power Low warning, media lane 5. Clear on Read	
	3	L-Rx4 Power Low war	ning	Rx input power Low warning, media lane 4. Clear on Read	
	2	L-Rx3 Power Low war	ning	Rx input power Low warning, media lane 3. Clear on Read	
	1	L-Rx2 Power Low war	ning	Rx input power Low warning, media lane 2. Clear on Read	
	0	L-Rx1 Power Low war	ning	Rx input power Low warning, media lane 1. Clear on Read	
Byte	Bit	Name	Descripti	on	Туре
153	7-0	Reserved			RO
154	7-0	Tx1 Power MSB	Internally	measured Tx output optical power: unsigned integer in 0.1	RO
155	7-0	Tx1 Power LSB	uW increm	nents, yielding a total measurement range of 0 to 6.5535	Opt.
156	7-0	Tx2 Power MSB	_ mW (~-40) to +8.2 dBm)	
157	7-0	Tx2 Power LSB			
158	7-0	Tx3 Power MSB			
159	7-0	Tx3 Power LSB			
160	7-0	Tx4 Power MSB			
161	7-0	Tx4 Power LSB			
162	7-0	Tx5 Power MSB]		
163	7-0	Tx5 Power LSB			
164	7-0	Tx6 Power MSB	1		
165	7-0	Tx6 Power LSB	1		
166	7-0	Tx7 Power MSB	1		
					1 1
167	7-0	Tx7 Power LSB	1		
167 168	7-0 7-0	Tx7 Power LSB Tx8 Power MSB	-		

multiLane	
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170	7-0	Tx1 Bias MSB	Internally measured Tx bias current monitor: unsigned integer in 2 uA	RO
171	7-0	Tx1 Bias LSB	increments, times the multiplier from Table 8-33.	Opt.
172	7-0	Tx2 Bias MSB		
173	7-0	Tx2 Bias LSB		
174	7-0	Tx3 Bias MSB		
175	7-0	Tx3 Bias LSB		
176	7-0	Tx4 Bias MSB		
177	7-0	Tx4 Bias LSB		
178	7-0	Tx5 Bias MSB		
179	7-0	Tx5 Bias LSB		
180	7-0	Tx6 Bias MSB		
181	7-0	Tx6 Bias LSB		
182	7-0	Tx7 Bias MSB		
183	7-0	Tx7 Bias LSB		
184	7-0	Tx8 Bias MSB		
185	7-0	Tx8 Bias LSB		
186	7-0	Rx1 Power MSB	Internally measured Rx input optical power:	RO
187	7-0	Rx1 Power LSB	unsigned integer in 0.1 uW increments, yielding a total measurement	Opt.
188	7-0	Rx2 Power MSB	range of 0 to 6.5535 mW (~-40 to +8.2 dBm)	
189	7-0	Rx2 Power LSB		
190	7-0	Rx3 Power MSB		
191	7-0	Rx3 Power LSB		
192				
	7-0	Rx4 Power MSB		
193	7-0 7-0	Rx4 Power MSB Rx4 Power LSB		
193 194	7-0 7-0 7-0	Rx4 Power MSBRx4 Power LSBRx5 Power MSB		
193 194 195	7-0 7-0 7-0 7-0	Rx4 Power MSBRx4 Power LSBRx5 Power MSBRx5 Power LSB		
193 194 195 196	7-0 7-0 7-0 7-0 7-0	Rx4 Power MSBRx4 Power LSBRx5 Power MSBRx5 Power LSBRx6 Power MSB		
193 194 195 196 197	7-0 7-0 7-0 7-0 7-0 7-0	Rx4 Power MSBRx4 Power LSBRx5 Power MSBRx5 Power LSBRx6 Power MSBRx6 Power LSB		
193 194 195 196 197 198	7-0 7-0 7-0 7-0 7-0 7-0 7-0	Rx4 Power MSBRx4 Power LSBRx5 Power MSBRx5 Power LSBRx6 Power MSBRx6 Power LSBRx7 Power MSB		
193 194 195 196 197 198 199	7-0 7-0 7-0 7-0 7-0 7-0 7-0 7-0	Rx4 Power MSBRx4 Power LSBRx5 Power MSBRx5 Power LSBRx6 Power MSBRx6 Power LSBRx7 Power MSBRx7 Power LSB		
193 194 195 196 197 198 199 200	7-0 7-0 7-0 7-0 7-0 7-0 7-0 7-0 7-0	Rx4 Power MSBRx4 Power LSBRx5 Power MSBRx5 Power LSBRx6 Power MSBRx6 Power MSBRx7 Power MSBRx7 Power MSBRx8 Power MSBRx8 Power MSB		

4.2 Interrupt Masks

Masks shown in this tab are used to prevent a specified flag of generating an interrupt (IntL) when asserted and prevent continued interruption from on-going conditions.

When a mask is set, an interrupt will not be asserted by the corresponding (Alarm/Warning) latched flag bit.

All Masking bits are volatile and will be reset (set to 0) on module startup.

State Changed Alarms RX Power X Bias TX Power Ch RX LOS TX LOS TX LOL TX Fault State Changed 1 RX Power X Bias TX Power 1 2 3 5 6 7 High Low High Low High Low	State Changed Harris Warning- Lanes pecific Flag Masks RX Power TX Blass RX Power TX Power<	Click to	refresh i	this pag	e	Refr	esh	Alarr	n Flag	s	_	-	_	_	_	-	_	_	_	-	_	
Lane Specific Flag Mads RX Power TX Bias TX Power TX Bias TX Power TX Bias TX Power Ch RX LOS TX LOS TX LOS TX Fault State Cheg Ch High Low High Low	Lane-Specific Flag Masks RX Power TK Bask TK Power TK	📃 State	Change	d				Ala	ms	_	_				Warr	nings			_			
Ch High Low High	Ch RM LOS TX LOL TX LOL TX LOL TX Fault State Chrig Ch High Low	Lane-Spec	ific Flag	Masks	_				RX F	ower	TX Bi	as	TX Po	wer		RX Po	wer	TXE	Bias	TX	ower	
	1 1	Ch RX LOS	TX LOS	RX LOL	TX LOL	TX Fault	State Chng	Ch	High	Low	High	Low	High	Low	Ch	High	Low	High	Low	High	Low	
	2 - - 2 -	1						1							1	1						
2 3 3 3 3 3 1 1 1 3 1	2 3 3 3 3 1 1 3 4 5 5 5 1 1 5 5 6 7 5 1 1 6 7 6 7 6 1 1 8 7 6 7 6 1 1 Hgh Low Hgh Low Hgh Low Hgh Low 1 VCC 3.3 AUX 3 VCC 3.3 AUX 3 1							2	P						2							
	3 4 4 4 4 5 5 5 5 5 6 6 6 6 6 7 7 7 7 7 8 7 8 7 7 7 Hgh Low Hgh Low Hgh Low Hgh Low Temp AUX 2 Temp AUX 2 VCC 3.3 AUX 3 VCC 3.3 AUX 3	2						3							3							
	4 5 5 5 5 6 7 6 7 7 7 8 7 7 8 7 8 7 7 High Low High Low High Low High Low Temp AUX 2 Temp AUX 2 VCC 3.3 AUX 3 VCC 3.3 AUX 3	3						4							4							
5 - - 6 -	5 6 6 6 7 6 7 7 7 7 8 7 8 8 7 High Low High Low High Low High Low Temp AUX 2 Temp AUX 2 VCC 3.3 AUX 3 VCC 3.3 AUX 3	4						5							5							
6 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	6 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	5						6							6							
7 8 High Low High Low	7 8 8 8 1 8 1	6						7							7							
8 High Low High Low High Low	8 High Low High Low Temp AUX 2 Temp AUX 2 VCC 3.3 AUX 3 VCC 3.3 AUX 3	7						8							8							
nigh Low nigh Low nigh Low	mage dow mage dow mage dow Temp AUX 2 AUX 2 VCC 3.3 AUX 3 VCC 3.3 AUX 3	8											111-6	1								
	VCC 3.3 AUX 3 VCC 3.3 AUX 3							То	-			IV 2	nign	LOW	Tou		ingn i	LOW	ALLY 3			
									C 3.3		AL	JX 3			VC	C 3.3			AUX 3			

Figure 3: Interrupt Masks Tab

multiLane

The table below shows the corresponding MSA mapping for the interrupt flags.

Byte	Bits	Name	Description	Туре
213	7	M- Data Path State Changed flag	Masking bit for Data Path State Changed flag, host lane 8	RW
		mask, host lane 8		RQD
	6	M-Data Path State Changed flag	Masking bit for Data Path State Changed flag, host lane 7]
		mask, host lane 7		
	5	M-Data Path State Changed flag	Masking bit for Data Path State Changed flag, host lane 6	
		mask, host lane 6		
	4	M-Data Path State Changed flag	Masking bit for Data Path State Changed flag, host lane 5	
		mask, host lane 5		_
	3	M-Data Path State Changed flag	Masking bit for Data Path State Changed flag, host lane 4	
		mask, host lane 4		-
	2	M-Data Path State Changed flag	Masking bit for Data Path State Changed flag, host lane 3	
		mask, host lane 3	Madia bit for Data Bath Chata Channed floor heat land 2	-
	1	M-Data Path State Changed flag	Masking bit for Data Path State Changed flag, host lane 2	
		M Data Dath State Changed flag	Macking hit for Data Dath Ctata Changed flag, host lang 1	-
	0	M-Data Path State Changed hag	Masking bit for Data Path State Changed hag, host lane 1	
214	7	M-Tyg Fault flag mack	Macking hit for Ty Fault flag, modia Jano 9	D\//
214	6	M-Tx7 Fault flag mask	Masking bit for Tx Fault flag, media Jano 7	Ont
	5	M-Tx6 Fault flag mask	Masking bit for Tx Fault flag, media lane 6	- ^{Opt.}
	1	M-Ty5 Fault flag mask	Masking bit for Tx Fault flag, media Jano 5	-
	3	M-Tx4 Fault flag mask	Masking bit for Tx Fault flag, media lane 3	-
	2	M-Tx3 Fault flag mask	Masking bit for Tx Fault flag, media lane 3	-
	1	M-Ty2 Fault flag mack	Masking bit for Tx Fault flag, media lane 3	-
		M-Tx1 Fault flag mask	Masking bit for Tx Fault flag, media lane 1	-
215	7	M-Tyg LOS flag mask	Masking bit for Tx LOS flag, Jano 8	D\//
215	6	M-Ty7 LOS flag mask	Masking bit for TX LOS flag, Jane 7	Ont
	5	M-Tx6 LOS flag mask	Masking bit for Tx LOS flag, Jane 6	1 ^{opt.}
	4	M-Tx5 LOS flag mask	Masking bit for Tx LOS flag, Jane 5	-
	3	M-Ty4 LOS flag mask	Masking bit for Tx LOS flag, lane 4	-
	2	M-Tx3 LOS flag mask	Masking bit for Tx LOS flag, Jane 3	-
	1	M-Tx2 LOS flag mask	Masking bit for Tx LOS flag, lane 2	-
	0	M-Tx1 LOS flag mask	Masking bit for Tx LOS flag, lane 1	-
216	7	M-Tx8 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 8	RW
	6	M-Tx7 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, Jane 7	Opt.
	5	M-Tx6 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 6	-
	4	M-Tx5 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 5	1
	3	M-Tx4 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 4	1
	2	M-Tx3 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 3	1
	1	M-Tx2 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 2	1
	0	M-Tx1 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 1	1
217	7	M-Tx8 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 8	RW
	6	M-Tx7 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 7	Opt.
	5	M-Tx6 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 6	1
	4	M-Tx5 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 5	1
	3	M-Tx4 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 4	1
	2	M-Tx3 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 3	1
	1	M-Tx2 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 2	1
	0	M-Tx1 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 1	
218	7	M-Tx8 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 8	RW
	6	M-Tx7 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 7	Opt.

	5.0			
nult	IL	ane		
		- V		
1 1	5	M-Tx6 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 6	1
	4	M-Tx5 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 5	1
	3	M-Tx4 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 4	1
	2	M-Tx3 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 3	1
	1	M-Tx2 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 2	1
	0	M-Tx1 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 1	1
219	7	M-Tx8 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 8	RW
	6	M-Tx7 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 7	Opt.
	5	M-Tx6 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 6	1
	4	M-Tx5 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 5	4
	3	M-Tx4 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 4	4
	2	M-Tx3 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 3	4
	1	M-1x2 Power Low Alarm flag mask	Masking bit for 1x output power Low Alarm, media lane 2	4
220	0	M-Tx1 Power Low Alarm flag mask	Masking bit for 1x output power Low Alarm, media lane 1	DIM
220	/	M-1x8 Power High Warning flag	Masking bit for Tx output power High Warning,	RW
	6	M Ty7 Dowor High Warping flag	Macking bit for Tx output newer High Warning	Opt.
	0	mask	masking bit for TX output power high warning, media lane 7	
	5	M-Tx6 Power High Warning flag	Masking hit for Tx output power High Warping	-
	5	mask	media lane 6	
	4	M-Tx5 Power High Warning flag	Masking bit for Tx output power High Warning,	1
		mask	media lane 5	
	3	M-Tx4 Power High Warning flag	Masking bit for Tx output power High Warning,	1
		mask	media lane 4	
	2	M-Tx3 Power High Warning flag	Masking bit for Tx output power High Warning,	
		mask	media lane 3	1
	1	M-Tx2 Power High Warning flag	Masking bit for Tx output power High Warning,	
	0	mask	media lane 2	4
	0	M-TX1 Power High Warning flag	Masking bit for Tx output power High Warning,	
221	7	Marching flag	Macking hit for Tx output newer Low Warning	DW/
221	/	mask	masking bit for TX output power Low Warning,	Opt
	6	M-Tx7 Power Low Warning flag	Masking bit for Tx output power Low Warping	opt.
	0	mask	media lane 7	
	5	M-Tx6 Power Low Warning flag	Masking bit for Tx output power Low Warning.	1
		mask	media lane 6	
	4	M-Tx5 Power Low Warning flag	Masking bit for Tx output power Low Warning,	1
		mask	media lane 5	
	3	M-Tx4 Power Low Warning flag	Masking bit for Tx output power Low Warning,	
		mask	media lane 4	4
	2	M-Tx3 Power Low Warning flag	Masking bit for Tx output power Low Warning,	
		mask	media lane 3	4
	1	M-1x2 Power Low Warning flag	Masking bit for Tx output power Low Warning,	
	0	M Ty1 Dowor Low Warping flag	Macking bit for Tx output newer Low Warping	-
	0	mack	masking bit for TX output power Low Warning,	
222	7	M-Tx8 Bias High Alarm flag mask	Masking hit for Tx hias High Alarm media lane 8	RW
222	6	M-Tx7 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 7	Opt.
	5	M-Tx6 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 6	
	4	M-Tx5 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 5	1
	3	M-Tx4 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 4	1
	2	M-Tx3 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 3	1
	1	M-Tx2 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 2	
	0	M-Tx1 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm media lane 1	

multiLane

223	7	M-Tx8 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 8	RW
	6	M-Tx7 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 7	Opt.
	5	M-Tx6 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 6	_
	4	M-Tx5 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 5	_
	3	M-1x4 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 4	4
	2	M-Tx3 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 3	4
	1	M-Tx2 Bias Low Alarm flag mask	Masking bit for Tx Bias Low Alarm, media lane 2	-
	0	M-Tx1 Bias Low Alarm flag mask	Masking bit for Tx Bias Low Alarm, media lane 1	
224	7	M-Tx8 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 8	RW
	6	M-Tx7 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 7	Opt.
	5	M-Tx6 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 6	_
	4	M-1x5 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 5	_
	3	M-Tx4 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 4	_
	2	M-Tx3 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 3	-
	1	M-1x2 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 2	_
	0	M-Tx1 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 1	
225	/	M-1x8 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 8	RW
	6	M-Tx/ Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 7	Opt.
	5	M-Tx6 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 6	_
	4	M-Tx5 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 5	_
	3	M-Tx4 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 4	4
	2	M-Tx3 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 3	4
	1	M-Tx2 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 2	4
	0	M-Tx1 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 1	
226	7	M-Rx8 LOS flag mask	Masking bit for Rx LOS flag, media lane 8	RW
	6	M-Rx7 LOS flag mask	Masking bit for Rx LOS flag, media lane 7	Opt.
	5	M-Rx6 LOS flag mask	Masking bit for Rx LOS flag, media lane 6	_
	4	M-Rx5 LOS flag mask	Masking bit for Rx LOS flag, media lane 5	_
	3	M-Rx4 LOS flag mask	Masking bit for Rx LOS flag, media lane 4	_
	2	M-Rx3 LOS flag mask	Masking bit for Rx LOS flag, media lane 3	_
	1	M-Rx2 LOS flag mask	Masking bit for Rx LOS flag, media lane 2	
	0	M-Rx1 LOS flag mask	Masking bit for Rx LOS flag, media lane 1	
227	7	M-Rx8 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 8	RW
	6	M-Rx7 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 7	Opt.
	5	M-Rx6 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 6	_
	4	M-Rx5 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 5	_
	3	M-Rx4 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 4	_
	2	M-Rx3 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 3	
	1	M-Rx2 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 2	_
	0	M-Rx1 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 1	
228	7	M-Rx8 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 8	RW
	6	M-Rx7 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 7	Opt.
	5	M-Rx6 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 6	4
	4	M-Rx5 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 5	4
	3	M-Rx4 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 4	4
	2	M-Rx3 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 3	4
	1	M-Rx2 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 2	4
	0	M-Rx1 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 1	
229	7	M-Rx8 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 8	RW
	6	M-Rx7 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 7	Opt.
	5	M-Rx6 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 6	
	4	M-Rx5 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 5	4
	3	M-Rx4 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 4	4
	2	M-Rx3 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 3	4
	1	M-Rx2 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 2	4
	0	M-Rx1 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 1	



		-		
33	7	M-Aux 2 Low Warning flag mask	Masking bit for Aux 2 monitor low warning flag	RW Opt.
	6	M-Aux 2 High Warning flag mask	Masking bit for Aux 2 monitor high warning flag	
	5	M-Aux 2 Low Alarm flag mask	Masking bit for Aux 2 monitor low alarm flag	
	4	M-Aux 2 High Alarm flag mask	Masking bit for Aux 2 monitor high alarm flag	
	3	M-Aux 1 Low Warning flag mask	Masking bit for Aux 1 monitor low warning flag	
	2	M-Aux 1 High Warning flag mask	Masking bit for Aux 1 monitor high warning flag	
	1	M-Aux 1 Low Alarm flag mask	Masking bit for Aux 1 monitor low alarm flag	
	0	M-Aux 1 High Alarm flag mask	Masking bit for Aux 1 monitor high alarm flag	
34	7	M-Vendor Defined Low Warning flag mask	Masking bit for Vendor defined low warning flag	RW Opt.
	6	M-Vendor Defined High Warning flag mask	Masking bit for Vendor defined high warning flag	
	5	M-Vendor Defined Low Alarm flag mask	Masking bit for Vendor defined low alarm flag	
	4	M-Vendor Defined High Alarm flag mask	Masking bit for Vendor defined high alarm flag	
	3	M-Aux 3 Low Warning flag mask	Masking bit for Aux 3 monitor low warning flag	
	2	M-Aux 3 High Warning	Masking bit for Aux 3 monitor high warning flag	
		flag mask		
	1	M-Aux 3 Low Alarm flag mask	Masking bit for Aux 3 monitor low alarm flag	
	0	M-Aux 3 High Alarm flag mask	Masking bit for Aux 3 monitor high alarm flag	
35	7-0	Reserved flag mask		
36	7-0	Custom	Module level flag masks	

4.3 Controls

The control fields allow the host to dynamically change the behavior of the device. It allows the user to control Tx Input Equalization, Rx amplitude, Rx Pre-Cursor and Rx Post-Cursor.

The User should follow this procedure:

multiLane

- Set values to the control fields.
- Apply the configuration by selecting either ApplyDataPathInit or ApplyImmmediate.
- Press one of the 2 buttons (Apply All or Apply Lane) depending on user need.
- The module copies the data to the Active set.
- If the DataPathPwrUp is set, this applied configuration will be applied to the hardware.

Also this tab allows the user to control the module voltage, in case of the MCB is supplied by dual supply (5V and 3.3V). Three voltage levels are available: 3.15V, 3.3V and 3.45V.



Host VCC					
Set Host VCC:	○ 3.15V	● 3.3V	○ 3.45V	Note: This option is effective if the host is powered by 5V only.	

Figure 4: MCB Voltage Control

	lasks Controls							
		linet.	100					
Click to refresh	this page Ref	resh Page		@ 2 2V	2 4EV Makes Thi	·	1	El contra
		Set Ho	SE VCC: () 3.15V	• 5.3V	3.45V Note: In	is option is effective if	the host is powered by	5v only.
Tx Output Disable	Tx Polarity Flip	Tx Squelch Disable	Tx Force Squelch	Tx Flag Squelch	Rx Polarity Flip	Rx Output Disable	Rx Squelch Disable	Rx Flag Squelch
Tx1	Tx1	Tx1	Tx1	Tx1	Rx1	Rx1	Rx1	Rx1
Tx2	Tx2	Tx2	Tx2	Tx2	Rx2	Rx2	Rx2	Rx2
Tx3	Tx3	Tx3	Tx3	Tx3	Rx3	Rx3	Rx3	Rx3
Tx4	Tx4	Tx4	Tx4	Tx4	Rx4	Rx4	Rx4	Rx4
Tx5	Tx5	Tx5	Tx5	Tx5	Rx5	Rx5	Rx5	Rx5
Tx6	Tx6	Tx6	Tx6	Tx6	Rx6	Rx6	Rx6	Rx6
Tx7	Tx7	Tx7	Tx7	Tx7	Rx7	Rx7	Rx7	Rx7
Tx8	Tx8	Tx8	Tx8	Tx8	Rx8	Rx8	Rx8	Rx8
Tx Input Equalization		Rx Output Amplitude	Rx Output Pre-cu	ursor	Rx Output Post-c	cursor	Apply Data	DataPathPwrUp
Tx1 U	0 dB	Rx1 mV	Rx1 U	0 dB	Rx1	0 dB	 ApplyDataPathInit 	Ch1
Tx2	0 dB		· · · · · ·		· · · · · ·		 ApplyImmediate 	Ch2
*** *********	0 00	mV	Rx2	0 00	Rx2		Apply Lape	Ch3
тхз 🔍	0 dB	Rx3 mV	Rx3 U	0 dB	Rx3	0 dB	Appry cane	Ch4
Tx4	0 dB	Rx4 mV	Rx4	0 dB	Rx4	0 dB	Apply All	Ch5
		Due						Ch6
1x5	0 08	mv mv	Rx5		Rx5			
Тхб 🔍	0 dB	Rx6 mV	Rx6	0 dB	Rx6	0 dB		CII0
Tx7 U	0 dB	Rx7 _ mV	Rx7	0 dB	Rx7 0	0 dB		
	0	Rx8 mV		0 dR	T			
1X8	dB	···· · · · · · · · · · · · · · · · · ·	Rx8	· · · ·	Rx8	U UB		

Figure 5: Control Tab

The following table shows the corresponding registers, along with their names and description.

Byte	Bit	Name	Description	Туре
128	7	DataPathDeinit Host Lane 8	Data Path initialization control for host lane 8	RW
			0b=Initialize the data path associated with host lane 8	RQD
			1b=Deinitialize the data path associated with host lane 8	
	6	DataPathDeinit Host Lane 7	Data Path initialization control for host lane 7	
			0b=Initialize the data path associated with host lane 7	
			1b=Deinitialize the data path associated with host lane 7	
	5	DataPathDeinit Host Lane 6	Data Path initialization control for host lane 6	
			0b=Initialize the data path associated with host lane 6	
			1b=Deinitialize the data path associated with host lane 6	
	4	DataPathDeinit Host Lane 5	Data Path initialization control for host lane 5	
			0b=Initialize the data path associated with host lane 5	
			1b= Deinitialize the data path associated with host lane 5	
	3	DataPathDeinit Host Lane 4	Data Path initialization control for host lane 4	
			0b=Initialize the data path associated with host lane 4	
			1b=Deinitialize the data path associated with host lane 4	
	2	DataPathDeinit Host Lane 3	Data Path initialization control for host lane 3	
			0b=Initialize the data path associated with host lane 4	
			1b=Deinitialize the data path associated with host lane 3	
	1	DataPathDeinit Host Lane 2	Data Path initialization control for host lane 2	
			0b=Initialize the data path associated with host lane 2	
			1b=Deinitialize the data path associated with host lane 2	
	0	DataPathDeinit Host Lane 1	Data Path initialization control for host lane 1	
			0b=Initialize the data path associated with host lane 1	
			1b=Deinitialize the data path associated with host lane 1	



129	7	Tx8 Polarity Flip	0b=No polarity flip for lane 8	RW
	6	Tx7 Polarity Flip	0b=No polarity flip for lane 7	Opt.
	0		1b=Tx input polarity flip for lane 7	
	5	Tx6 Polarity Flip	0b=No polarity flip for lane 6	
	5	The Folding Flip	1b=Tx input polarity flip for lane 6	
	4	Tx5 Polarity Flip	0h=No polarity flip for lane 5	
		TX5 Folding Thp	1b=Tx input polarity flip for lane 5	
	3	Tx4 Polarity Flip	0b=No polarity flip for lane 4	
	0	TXTT oldricy Thp	1b=Tx input polarity flip for lane 4	
	2	Tx3 Polarity Flip	Ob=No polarity flip for lane 3	
	2	The Foldiney Flip	1b=Tx input polarity flip for lane 3	
	1	Tx2 Polarity Flip	0b=No polarity flip for lane 2	
	-	The Foldiney Flip	1b=Tx input polarity flip for lane 2	
	0	Tx1 Polarity Flip	0b=No polarity flip for lane 1	
	Č.	int i orancy i np	1b=Tx input polarity flip for lane 1	
130	7	Tx8 Disable	0b=Tx output enabled for media lane 8	RW
100		The Bloable	1b=Tx output disabled for media lane 8	Opt.
	6	Tx7 Disable	0b=Tx output enabled for media lane 7	
	•		1b=Tx output disabled for media lane 7	
	5	Tx6 Disable	0b=Tx output enabled for media lane 6	
	5	The bloable	1h=Tx output disabled for media lane 6	
	4	Tx5 Disable	0b=Tx output enabled for media lane 5	
		TAS DISubic	1h=Tx output disabled for media lane 5	
	3	Tx4 Disable	0h=Tx output enabled for media lane 4	
		TAT DISubic	1b=Tx output disabled for media lane 4	
	2	Tx3 Disable	Ob=Tx output enabled for media lane 3	
	2		1h=Tx output disabled for media lane 3	
ı F	1	Tv2 Disable	0h=Tx output enabled for media lane 2	
	1	TAZ DISODIE	1h=Tx output disabled for media lane 2	
	0	Tv1 Disable	0h=Tx output enabled for media lane 1	
	0	TAT DISuble	1h=Tx output disabled for media lane 1	
131	7	Tx8 Squelch Disable	0h=Tx output squelch permitted for media lane 8 when	RW
101	'	TX0 Squelet Disuble	associated host input LOS is detected	Opt
			1b=Tx output squelch not permitted for media lane 8	opa
	6	Tx7 Squelch Disable	0h=Tx output squeich net permitted for media lane 7 when	
	0	TX7 Oquelen Disuble	associated host input LOS is detected	
			1b=Tx output squelch not permitted for media lane 7	
	5	Tx6 Squelch Disable	0b=Tx output squeich permitted for media lane 6 when	
		The equelent blouble	associated host input LOS is detected	
			1b=Tx output squelch not permitted for media lane 6	
	4	Tx5 Squelch Disable	0b=Tx output squeich permitted for media lane 5 when	
		The equelent bloable	associated host input LOS is detected	
			1b=Tx output squelch not permitted for media lane 5	
	3	Tx4 Squelch Disable	0b=Tx output squelch permitted for media lane 4 when	
	-		associated host input LOS is detected	
			1b=Tx output squelch not permitted for media lane 4	
	2	Tx3 Squelch Disable	0b=Tx output squelch permitted for media lane 3 when	
	-		associated host input LOS is detected	
			1b=Tx output squelch not permitted for media lane 3	
	1	Tx2 Squelch Disable	0b=Tx output squelch permitted for media lane 2 when	
	-		associated host input LOS is detected	
			1b=Tx output squelch not permitted for media lane 2	
, L	0	Ty1 Squelch Disable	0b=Tx output squelch permitted for media lane 1 when	—
	()			1
	0	TXI Squeich Disuble	associated host input LOS is detected	

22 📩 multilaneinc.com



132	7	Tx8 Force Squelch	0b=No impact on Tx behavior for media lane 8	RW
			1b=1x output squeiched for media lane 8	Opt.
	6	Tx7 Force Squelch	0b=No impact on Tx behavior for media lane 7	
			1b=Tx output squelched for media lane 7	
	5	Tx6 Force Squelch	0b=No impact on Tx behavior for media lane 6	
			1b=Tx output squelched for media lane 6	
	4	Tx5 Force Squelch	0b=No impact on Tx behavior for media lane 5	
			1b=Tx output squelched for media lane 5	
	3	Tx4 Force Squelch	0b=No impact on Tx behavior for media lane 4	
			1b=Tx output squelched for media lane 4	
	2	Tx3 Force Squelch	Ob=No impact on Tx behavior for media lane 3	-
	-	into i orce oqueleri	1b=Tx output squelched for media lane 3	
	1	Ty2 Force Squalch	0b-No impact on Ty behavior for modia Jano 2	-
	1	TX2 TOICE Squeich	th=Ty output squalshed for media lane 2	
	0	Tut Farra Caualah	1D-1X output squeicheu for media lane 2	-
	0	TX1 Force Squeich	UD=INO IMpact on TX benavior for media lane 1	
			1b=1x output squeiched for media lane 1	
133	/:0	Reserved		RO
134	7	Tx8 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 8	RW
			1b=Tx input eq adaptation frozen at last value for lane 8	Opt.
	6	Tx7 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 7	
			1b=Tx input eq adaptation frozen at last value for lane 7	
	5	Tx6 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 6	-
	-		1b=Tx input eq adaptation frozen at last value for lane 6	
	4	Tv5 Input Eq Adaptation Froozo	0b- No impact on Ty input or adaptation behavior for lang 5	
	7	TX5 Input Eq Adaptation Treeze	th=Tv input or adaptation frozon at lact value for lane 5	
	2	Tud Innut Fo Adaptation France	1D-1X input eq adaptation nozen at last value for lane 5	-
	3	TX4 Input Eq Adaptation Freeze	UD= No Impact on TX input eq adaptation behavior for lane 4	
		TALLE	ID= IX Input eq adaptation frozen at last value for lane 4	
	2	Tx3 Input Eq Adaptation Freeze	0b= No impact on 1x input eq adaptation behavior for lane 3	
			1b=Tx input eq adaptation frozen at last value for lane 3	_
	1	Tx2 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 2	
			1b=Tx input eq adaptation frozen at last value for lane 2	
	0	Tx1 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 1	
			1b=Tx input eq adaptation frozen at last value for lane 1	
135	7-6	Tx4 Input Eq Adaptation Store	Tx Input Eq Adaptation Store location	WO
	5-4	Tx3 Input Eq Adaptation Store	00b=reserved	Opt.
	3-2	Tx2 Input Eq Adaptation Store	01b=store location 1	
	1-0	Tx1 Input Eq Adaptation Store	10b=store location 2	
	10	TAT Input Eq Adaptation Store	11b=reserved	
			See section 6.2.4.4	
136	7-6	Tx8 Input Eq Adaptation Store	Tx Input Eq Adaptation Store location	WO
100	5-4	Tx7 Input Eq Adaptation Store	00h=reserved	Opt
	27	Tyo Input Eq Adaptation Store	01h=store location 1	opt.
	3-2	TVE Input En Adoptation Store	10h=store location 2	
	1-0	TX5 Input Eq Adaptation Store	11b=score location 2	
			Son soction 6.2.4.4	
4.0.7	_			
137	7	Kx8 Polarity Flip	Ub=No polarity flip for lane 8	RW
			1b=Rx output polarity flip for lane 8	Opt.
	6	Rx7 Polarity Flip	0b=No polarity flip for lane 7	
			1b=Rx output polarity flip for lane 7	
	5	Rx6 Polarity Flip	0b=No polarity flip for lane 6	
			1b=Rx output polarity flip for lane 6	
	4	Rx5 Polarity Flip	0b=No polarity flip for lane 5	7
	•	· · · · · · · · · · · · · · · · · · ·	1b=Rx output polarity flip for lane 5	
	2	Rx4 Polarity Flip	0h=No polarity flip for lane 4	-
	5		th=Rx output polarity flip for lang 4	
	2	Dv2 Delarity Elin	Ob-No polority flip for long 2	-
	2	KX5 Polarity Flip	bu-ivo polarity nipitori ane s	
		Dig Delevite St	1D=KX output polarity flip for lane 3	-
	1	KXZ Polarity Flip	up=ino polarity flip for lane 2	
			1b=Rx output polarity flip for lane 2	4
	0	Rx1 Polarity Flip	0b=No polarity flip for lane 1	
			1b=Rx output polarity flip for lane 1	



138	7	Rx8 Output Disable	0b=Rx output enabled for lane 8	RW
			1b=Rx output disabled for lane 8	Opt.
	6	Rx7 Output Disable	0b=Rx output enabled for lane 7	
			1b=Rx output disabled for lane 7	
	5	Rx6 Output Disable	0b=Rx output enabled for lane 6	
			1b=Rx output disabled for lane 6	
	4	Rx5 Output Disable	0b=Rx output enabled for lane 5	
			1b=Rx output disabled for lane 5	
	3	Rx4 Output Disable	0b=Rx output enabled for lane 4	
			1b=Rx output disabled for lane 4	
	2	Rx3 Output Disable	0b=Rx output enabled for lane 3	
			1b=Rx output disabled for lane 3	
	1	Rx2 Output Disable	0b=Rx output enabled for lane 2	
			1b=Rx output disabled for lane 2	
	0	Rx1 Output Disable	0b=Rx output enabled for lane 1	
			1b=Rx output disabled for lane 1	
139	7	Rx8 Squelch Disable	0b=Rx output squelch permitted for lane 8	RW
			1b=Rx output squelch not permitted for lane 8	Opt.
	6	Rx7 Squelch Disable	0b=Rx output squelch permitted for lane 7	
			1b=Rx output squelch not permitted for lane 7	
	5	Rx6 Squelch Disable	0b=Rx output squelch permitted for lane 6	
			1b=Rx output squelch not permitted for lane 6	
	4	Rx5 Squelch Disable	0b=Rx output squelch permitted for lane 5	
			1b=Rx output squelch not permitted for lane 5	
	3	Rx4 Squelch Disable	0b=Rx output squelch permitted for lane 4	
			1b=Rx output squelch not permitted for lane 4	
	2	Rx3 Squelch Disable	0b=Rx output squelch permitted for lane 3	
			1b=Rx output squelch not permitted for lane 3	
	1	Rx2 Squelch Disable	0b=Rx output squelch permitted for lane 2	
			1b=Rx output squelch not permitted for lane 2	
	0	Rx1 Squelch Disable	0b=Rx output squelch permitted for lane 1	
			1b=Rx output squelch not permitted for lane 1	

The optional controls follow this flow diagram.



Figure 6: Control Set Data Flow Diagram



143	7	Staged Set 0 Lane 8 Apply_DataPathInit	1b=Apply Stag	ed Control Set 0 lane 8 settings using DataPathInit	WO RQD			
	6	Staged Set 0 Lane 7 Apply_DataPathInit	1b=Apply Stag	ed Control Set 0 lane 7 settings using DataPathInit				
	5	Staged Set 0 Lane 6 Apply_DataPathInit	1b=Apply Stag	ed Control Set 0 lane 6 settings using DataPathInit				
	4	Staged Set 0 Lane 5 Apply_DataPathInit	1b=Apply Stag	jed Control Set 0 lane 5 settings using DataPathInit				
	3	Staged Set 0 Lane 4 Apply_DataPathInit	1b=Apply Stag	1b=Apply Staged Control Set 0 lane 4 settings using DataPathInit				
	2	Staged Set 0 Lane 3 Apply_DataPathInit	1b=Apply Stag	ed Control Set 0 lane 3 settings using DataPathInit				
	1	Staged Set 0 Lane 2 Apply_DataPathInit	1b=Apply Stag	jed Control Set 0 lane 2 settings using DataPathInit				
	0	Staged Set 0 Lane 1 Apply_DataPathInit	1b=Apply Stag	jed Control Set 0 lane 1 settings using DataPathInit				
144	7	Staged Set 0 Lane 8 Apply_Immediate	1b=Apply Stag State transition	jed Control Set 0 lane 8 settings with no Data Path ns	WO RQD			
	6	Staged Set 0 Lane 7 Apply_Immediate	1b=Apply Stag State transition	ged Control Set 0 lane 7 settings with no Data Path	_			
	5	Staged Set 0 Lane 6 Apply_Immediate	1b=Apply Stag State transition	Jed Control Set 0 lane 6 settings with no Data Path	_			
	4	Staged Set 0 Lane 5 Apply_Immediate	1b=Apply Stag State transition	jed Control Set 0 lane 5 settings with no Data Path ns				
	3	Staged Set 0 Lane 4 Apply_Immediate	1b=Apply Stag State transition	jed Control Set 0 lane 4 settings with no Data Path ns				
	2	Staged Set 0 Lane 3 Apply_Immediate	1b=Apply Stag State transition	jed Control Set 0 lane 3 settings with no Data Path ns				
	1	Staged Set 0 Lane 2 Apply_Immediate	1b=Apply Stag State transition	jed Control Set 0 lane 2 settings with no Data Path ns				
	0	Staged Set 0 Lane 1 Apply Immediate	1b=Apply Stag State transition	ed Control Set 0 lane 1 settings with no Data Path ns				
145	7-4	Staged Set 0 Lane 1 Aps	Sel code	ApSel code from Table 8-13 or Table 8-39, lane 1	RW			
	3-1	Staged Set 0 Lane 1 Dat	ta Path ID	First lane of the data path containing lane 1	RQD			
	0	Staged Set 0 Lane 1 Exp	olicit Control	0b=Use Application-defined settings for lane 1 1b=use Staged Set 0 control values for lane 1				
146	7-4	Staged Set 0 Lane 2 Ap	Sel code	ApSel code from Table 8-13 or Table 8-39 Jane 2	RW			
	3-1	Staged Set 0 Lane 2 Dat	ta Path ID	First lane of the data path containing lane 2 000b=Lane 1, 001b=Lane 2	RQD			
	0	Staged Set 0 Lane 2 Exp	olicit Control	0b=Use Application-defined settings for lane 2 1b=use Staged Set 0 control values for lane 2				
147	7-4	Staged Set 0 Lane 3 Aps	Sel code	ApSel code from Table 8-13 or Table 8-39, lane 3	RW			
	3-1	Staged Set 0 Lane 3 Dat	ta Path ID	First lane of the data path containing lane 3 000b=Lane 1, 001b=Lane 2, etc.	RQD			
	0	Staged Set 0 Lane 3 Exp	olicit Control	0b=Use Application-defined settings for lane 3 1b=use Staged Set 0 control values for lane 3				
148	7-4	Staged Set 0 Lane 4 Aps	Sel code	ApSel code from Table 8-13 or Table 8-39, lane 4	RW			
	3-1	Staged Set 0 Lane 4 Dat	ta Path ID	First lane of the data path containing lane 4 000b=Lane 1, 001b=Lane 2, etc.	RQD			
	0	Staged Set 0 Lane 4 Exp	olicit Control	0b=Use Application-defined settings for lane 4 1b=use Staged Set 0 control values for lane 4				
149	7-4	Staged Set 0 Lane 5 Aps	Sel code	ApSel code from Table 8-13 or Table 8-39, lane 5	RW			
	3-1	Staged Set 0 Lane 5 Dat	a Path ID	First lane of the data path containing lane 5 000b=Lane 1, 001b=Lane 2, etc.	RQD			
	0	Staged Set 0 Lane 5 Exp	olicit Control	0b=Use Application-defined settings for lane 5 1b=use Staged Set 0 control values for lane 5				
150	7-4	Staged Set 0 Lane 6 Aps	Sel code	ApSel code from Table 8-13 or Table 8-39, lane 6	RW			
	3-1	Staged Set 0 Lane 6 Dat	ta Path ID	First lane of the data path containing lane 6 000b=Lane 1, 001b=Lane 2, etc.	RQD			
	0	Staged Set 0 Lane 6 Exp	olicit Control	0b=Use Application-defined settings for lane 6 1b=use Staged Set 0 control values for lane 6				



151	7-4	Staged Set 0 Lane 7 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 7	RW
	3-1	Staged Set 0 Lane 7 Data Path ID	First lane of the data path containing lane 7	RQD
			000b=Lane 1, 001b=Lane 2, etc.	
	0	Staged Set 0 Lane 7 Explicit Control	Ob=Use Application-defined settings for lane 7	
			1b=use Staged Set 0 control values for lane 7	
152	7-4	Staged Set 0 Lane 8 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 8	RW
	3-1	Staged Set 0 Lane 8 Data Path ID	First lane of the data path containing lane 8	RQD
			000b=Lane 1, 001b=Lane 2, etc.	-
	0	Staged Set 0 Lane 8 Explicit Control	0b=Use Application default settings for lane 8	
			1b=use Staged Set 0 control values for lane 8	
153	7	Staged Set 0 Tx8	1b=Enable	RW
		Adaptive Input Eq Enable	0b=Disable (use manual fixed EQ)	Req
	6	Staged Set 0 Tx7	1b=Enable	
		Adaptive Input Eq Enable	0b=Disable (use manual fixed EQ)	
	5	Staged Set 0 Tx6	1b=Enable	1
		Adaptive Input Eq Enable	0b=Disable (use manual fixed EQ)	
	4	Staged Set 0 Tx5	1b=Enable	
		Adaptive Input Eq Enable	0b=Disable (use manual fixed EQ)	
	3	Staged Set 0 Tx4	1b=Enable	
		Adaptive Input Eq Enable	0b=Disable (use manual fixed EQ)	
	2	Staged Set 0 Tx3	1b=Enable	
		Adaptive Input Eq Enable	0b=Disable (use manual fixed EQ)	
	1	Staged Set 0 Tx2	1b=Enable	
		Adaptive Input Eq Enable	0b=Disable (use manual fixed EQ)	
	0	Staged Set 0 Tx1	1b=Enable	
		Adaptive Input Eq Enable	0b=Disable (use manual fixed EQ)	
154	7-6	Staged Set 0 Tx4	Recall stored Tx Eq adaptation value,	RW
		Adaptive Input Eq Recall	00b=do not Recall	Req
	5-4	Staged Set 0 Tx3	01b=store location 1	
		Adaptive Input Eq Recall	10D=store location 2	
	3-2	Staged Set 0 1X2	11D=reserved	
	1.0	Adaptive Input Eq Recall	See Section 0.2.4.4 for Store/Recail methodology	
	1-0	Adaptive Input Ed Decall		
155	7-6	Staged Set 0 Tv9	Pocall stored Ty Eq adaptation value	DW/
155	7-0	Adaptivo Input Ed Pocall	Ob-do pot Pocall	Rog
	5-4	Stagod Sot 0 Ty7	01b=store location 1	Ney
	57	Adaptive Input Fa Recall	10b=store location 2	
	3-2	Staged Set 0 Tx6	11b=reserved	
	52	Adaptive Input Fg Recall	See section 6.2.4.4 for Store/Recall methodology	
	1-0	Staged Set 0 Tx5		
	10	Adaptive Input Eq Recall		
156	7-4	Staged Set 0 Tx2 Input Eg control	Manual fixed Tx input eq control (See Table 6-4)	RW
	3-0	Staged Set 0 Tx1 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	Reg
157	7-4	Staged Set 0 Tx4 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	RW
	3-0	Staged Set 0 Tx3 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	Req
158	7-4	Staged Set 0 Tx6 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	RW
	3-0	Staged Set 0 Tx5 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	Req
159	7-4	Staged Set 0 Tx8 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	RW
	3-0	Staged Set 0 Tx7 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	Req
160	7	Staged Set 0 Tx8 CDR control	1b=CDR enabled, 0b=CDR bypassed	RW
	6	Staged Set 0 Tx7 CDR control	1b=CDR enabled, 0b=CDR bypassed	Req
	5	Staged Set 0 Tx6 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	4	Staged Set 0 Tx5 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	3	Staged Set 0 Tx4 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	2	Staged Set 0 Tx3 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	1	Staged Set 0 Tx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	0	Staged Set 0 Tx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	

multiLane

161	7	Staged Set 0 Rx8 CDR control	1b=CDR enabled, 0b=CDR bypassed	RW
	6	Staged Set 0 Rx7 CDR control	1b=CDR enabled, 0b=CDR bypassed	Opt.
	5	Staged Set 0 Rx6 CDR control	1b=CDR enabled, 0b=CDR bypassed]
	4	Staged Set 0 Rx5 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	3	Staged Set 0 Rx4 CDR control	1b=CDR enabled, 0b=CDR bypassed]
	2	Staged Set 0 Rx3 CDR control	1b=CDR enabled, 0b=CDR bypassed]
	1	Staged Set 0 Rx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	0	Staged Set 0 Rx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	
162	7-4	Staged Set 0 Rx2 Output Eq control, pre-cursor	Rx output equalization pre-cursor ¹	RW
	3-0	Staged Set 0 Rx1 Output Eq control, pre-cursor	Rx output equalization pre-cursor ¹	Opt.
163	7-4	Staged Set 0 Rx4 Output Eq control, pre-cursor	Rx output equalization pre-cursor ¹	RW
	3-0	Staged Set 0 Rx3 Output Eq control, pre-cursor	Rx output equalization pre-cursor ¹	Opt.
164	7-4	Staged Set 0 Rx6 Output Eq control, pre-cursor	Rx output equalization pre-cursor ¹	RW
	3-0	Staged Set 0 Rx5 Output Eq control, pre-cursor	Rx output equalization pre-cursor ¹	Opt.
165	7-4	Staged Set 0 Rx8 Output Eq control, pre-cursor	Rx output equalization pre-cursor ¹	RW
	3-0	Staged Set 0 Rx7 Output Eq control, pre-cursor	Rx output equalization pre-cursor ¹	Opt.
166	7-4	Staged Set 0 Rx2 Output Eq control, post-cursor	Rx output equalization post-cursor ¹	RW
	3-0	Staged Set 0 Rx1 Output Eq control, post-cursor	Rx output equalization post-cursor ¹	Opt.
167	7-4	Staged Set 0 Rx4 Output Eq control, post-cursor	Rx output equalization post-cursor ¹	RW
	3-0	Staged Set 0 Rx3 Output Eq control, post-cursor	Rx output equalization post-cursor ¹	Opt.
168	7-4	Staged Set 0 Rx6 Output Eq control, post-cursor	Rx output equalization post-cursor ¹	RW
	3-0	Staged Set 0 Rx5 Output Eq control, post-cursor	Rx output equalization post-cursor ¹	Opt.
169	7-4	Staged Set 0 Rx8 Output Eq control, post-cursor	Rx output equalization post-cursor ¹	RW
	3-0	Staged Set 0 Rx7 Output Eq control, post-cursor	Rx output equalization post-cursor ¹	Opt.
170	7-4	Staged Set 0 Rx2 Output Amplitude control	Rx output amplitude ²	RW
	3-0	Staged Set 0 Rx1 Output Amplitude control	Rx output amplitude ²	Opt.
171	7-4	Staged Set 0 Rx4 Output Amplitude control	Rx output amplitude ²	RW
	3-0	Staged Set 0 Rx3 Output Amplitude control	Rx output amplitude ²	Opt.
172	7-4	Staged Set 0 Rx6 Output Amplitude control	Rx output amplitude ²	RW
	3-0	Staged Set 0 Rx5 Output Amplitude control	Rx output amplitude ²	Opt.
173	7-4	Staged Set 0 Rx8 Output Amplitude control	Rx output amplitude ²	RW
	3-0	Staged Set 0 Rx7 Output Amplitude control	Rx output amplitude ²	Opt.

4.4 Low Speed Signals

This tab allows to control and monitor the HW signals, depending on the selected device. The sections below define the control signals for each group of devices that share the same HW signals, separately.

4.4.1 QDD Family

This family includes MCBs like ML4062-MCB, ML4062-MCB-MXP and ML4062-TR.

Module Input signals:

LPMode:

- If set to Low: Module is in High Power Mode
- If set to High: Module is in Low Power Mode

ResetL:

- If set to Low: Module is in Reset state
- If set to High: Module is out of Reset state

ModSelL:

- If set to Low: Module is selected and I2C communication is active
- If set to High: Module is not selected and I2C communication is inactive



Module Output signals:

IntL:

- If Read Low: interrupt source is present
- If Read High: no interrupt source is present

ModPrsL:

- If Read Low: Module is physically present
- If Read High: Module is physically absent

Get button is used to read the current state of these signals.



Figure 7: QDD HW Signals

4.4.2 OSFP Family

This family includes MCBs like ML4064-MCB, ML4064-TR.

Module Input signals:

LPWn:

- If set to Low: Module is in Low Power Mode
- If set to High: Module is in High Power Mode

RSTn:

- If set to Low: Module is in Reset State
- If set to High: Module is out of Reset State

Module Output signals:

PRSn:

- If Read Low: Module is physically present
- If Read High: Module is physically absent

INT:

- If Read Low: interrupt source is present
- If Read High: no interrupt source is present



Module Input	Module Output
LPWn	PRSn
RSTn	
Get	Get

Figure 8: OSFP HW Signals

4.4.3 DSFP Family

The DSFP family includes the ML4019-MCB board.

The control signals of this family are similar to those in OSPF. Refer to section 5.4.2 for more details.

4.4.4 QSFP Family

This includes MCB like ML4041K.

Module Input signals:

LPMode:

- If set to Low: Module is in High Power Mode
- If set to High: Module is in Low Power Mode

ResetL:

- If set to Low: Module is in Reset state
- If set to High: Module is out of Reset state

ModSelL:

- If set to Low: Module is selected and I2C communication is active
- If set to High: Module is not selected and I2C communication is inactive

Module Output signals:

IntL:

- If Read Low: interrupt source is present
- If Read High: no interrupt source is present

ModPrsL:

- If Read Low: Module is physically present
- If Read High: Module is physically absent



Figure 9: QSFP HW Signals



4.4.5 SFP-DD Family

This includes MCB like ML4022-MCB.

Module Input signals:

LPMode:

- If set to Low: Module is in High Power Mode
- If set to High: Module is in Low Power Mode

TxDisable0/ TxDisable1:

• Set to Low or High by the user for CH0 and CH1 respectively

Module Output signals:

TxFault0/TxFault1:

Output state (Low or High) from the Module for CH0 and CH1 respectively

RXLOS0/RXLOS1:

Output state (Low or High) from the Module for CH0 and CH1 respectively

User should click on **Refresh** button to get the current output signals state.

Rate Select HW Control Contacts:

Speed0-1/ Speed 1-1:

Set the rate of the Receiver for CH0 and CH1 respectively

Speed0-2/ Speed 1-2:

• Set the rate of the Transmitter for CH0 and CH1 respectively

Reserved Pins:

RSVD / RSVD2:

- As Output: pins are set to High or Low
- As Input: Pins are Tri-stated



Figure 10: SFP-DD HW Signals



4.5 Identification

The Identification tab summarizes module specifications, vendor information and others.

Controls Low Speed Signals Identification			
Refresh Page	Cable Length		
Specifications Identifier Power Class CLEI Connector type Device Technology Wavelength Wavelength Tol. Max Case Power Wavelength control Cooling Tunable	Cable Length Single Mode Fiber Length (OM5) Length (OM4) Length (OM3 50µm) Length (OM2 50 µm) Length (Copper) Vendor Name OUI Part Number Revision Serial Number Date Code		
	 Lot Code Vendor Specific		

Figure 11: Identification Tab

The following table shows the corresponding ID registers, along with their names and description.

Address	Size (bytes)	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power	
		characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-209	6	Copper Cable Attenuation	
210-211	2	Cable Assembly Lane	
		Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	



4.6 Options Available

This tab specifies the options implemented in the module.

Monitor					Options Availa	ble Load/Save MSA		
	Click	to refresh this p	oage	Refresh				
	Exte	nded Ethernet (Compliance Codes:					
		Rx Optical Pov	ver Measurement Type	:		Rx CDR Loss of Lock (LC	DL) Flag implemented	
		Rx output amp	olitude implemented			Rx Loss of Signal imple	mented	
		Tx Squelch im	plemented			Rx Optical Power Monit	or implemented	
		Tx Force Sque	lch implemented			Tx Optical Power Chan	nel Monitoring implemented	
		Tx Squelch Dis	able Implemented			Tx Bias Monitor implem	ented	
		Tx Disable im	plemented			Tx adaptive Equalization	on implemented	
		Tx polarity fli	p implemented			Tx input Equalization in	nplemented	
		Rx Squelch Di	sable implemented			Tx CDR Bypass impleme	ented	
		Rx Output Dis	able implemented			Tx CDR implemented		
		Rx polarity fli	p implemented			Staged Set 1 implemen	ted	
		Tx CDR Loss o	f Lock (LOL) Flag imp	lemented		Rx Output Control impl	emented	
		Tx LOS Flag in	mplemented			Rx CDR Bypass implem	ented	
		Tx Fault Flag	implemented			Rx CDR implemented		

Figure 12: Options Available Tab

The following table shows the corresponding registers, along with their names and description.

151	7	Detector type	0b=PIN detector	RO
			1b=APD detector	RQD
	6-5	Rx Output Eq type	00b=Peak-to-peak amplitude stays constant, or not]
			implemented, or no information	
			01b=Steady-state amplitude stays constant	
			10b=Average of peak-to-peak and steady-state amplitude stays	
			constant	
			11b=Reserved	
2	4	Rx Optical Power	0b=OMA	
		Measurement type	1b=average power	
	3	Rx LOS type	0b=Rx LOS responds to OMA	1
		87.037	1b=Rx LOS responds to Pave	
	2	Rx LOS fast mode	0b=Rx LOS fast mode not implemented	1
		implemented	1b=Rx LOS fast mode implemented	
			Refer to form factor hardware specification for timing	
			requirements	
	1	Tx Disable fast mode	0b=Tx Disable fast mode not implemented	
		implemented	1b=Tx Disable fast mode implemented	
			Refer to form factor hardware specification for timing	
			requirements	
	0	Module-Wide Tx Disable	0b=Tx Disable implemented per lane	1
	10100		1b=Any Tx Disable control bit being set disables all Tx lanes	



152	7-0	Per lane CDR Power saved Minimum power consumption saved per CDR per lane when placed in CDR bypass in multiples of 0.01 W rounded up to the next whole multiple of 0.01 W				
153	7	Rx Output Amplitude code 0011b implemented ¹	0b= 1b=	Amplitude code 0011b not implemented Amplitude code 0011b implemented	RO Opt.	
	6	Rx Output Amplitude code	0b=	Amplitude code 0010b not implemented		
1	5	Rx Output Amplitude code	0b=	0b=Amplitude code 0001b not implemented		
		0001b implemented ¹	1b=	Ib=Amplitude code 0001b implemented		
	4	Rx Output Amplitude code	0b=	Amplitude code 0000b not implemented]	
	2.0	0000b implemented ¹	1b=	Amplitude code 0000b implemented	-	
	3-0	Max Tx Input Eq	Tx II (see	mum supported value of the nput Equalization control for manual/fixed programming. section 6.2.4.1)		
154	7-4	Max Rx Output Eq	Maxi	imum supported value of the	RO	
		Post-cursor	Rx C	Dutput Eq Post-cursor control. (see section 6.2.4.2)	Opt.	
	3-0	Max Rx Output Eq Pre-	Maxi	imum supported value of the]	
		cursor	Rx Output Eq Pre-cursor control (see section 6.2.4.2)			
Byte	Bit	Name		Description	Туре	
155	/	wavelength control impleme	ented	UD=NO Wavelength control	RO	
	6	Tunable transmitter		0b=Transmitter not tunable	RQD	
	U U	implemented		1b=Transmitter tunable (page 04h and bank page 12h		
				shall be implemented)		
	5-4	Tx Squelch implemented		00b=Tx Squelch not implemented	1	
				01b=Tx Squelch reduces OMA		
				10b=Tx Squelch reduces Pave		
				11b=User control, both OMA and Pave squelch supported.		
	2	Ty Force Squalch implement	tod	(see Table 8-7)	-	
	5	TX Force squeich implement	teu	1b=Tx Force Squelch implemented		
	2	Tx Squelch Disable impleme	nted	0b=Tx Squelch Disable not implemented	1	
Deather	Bit	Name		Description	Turne	
вуте		Name		Description	Type	
Вуте	Die	Name		1b=Tx Squelch Disable implemented	Туре	
вуте	1	Tx Disable implemented		1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented	Туре	
Вуте	1 0	Tx Disable implemented Tx Polarity Flip implemented		1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented	Туре	
156	1 0 7-3	Tx Disable implemented Tx Polarity Flip implemented Reserved		1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented	RO RQD	
вуте 156	1 0 7-3 2	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented	nted	1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented	RO RQD RQD RQD	
вуте 156	1 0 7-3 2 1	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented	nted	Description 1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented 0b=Rx Disable not implemented	RO RQD RO RQD RQD	
вуте 156	1 0 7-3 2 1	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented	nted	Description 1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented 0b=Rx Disable not implemented 1b=Rx Disable not implemented 1b=Rx Disable not implemented	RO RQD RQD RQD	
вуте 156	1 0 7-3 2 1 0	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented Rx Disable implemented Rx Polarity Flip implemented	nted	1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 1b=Rx Disable not implemented 0b=Rx Polarity Flip not implemented 0b=Rx Polarity Flip not implemented	RO RO RQD RO RQD	
156	1 0 7-3 2 1 0	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented Rx Disable implemented Rx Polarity Flip implemented	nted	1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 0b=Rx Squelch Disable implemented 0b=Rx Disable not implemented 0b=Rx Disable implemented 0b=Rx Polarity Flip not implemented 0b=Rx Polarity Flip implemented	RO RQD RQD RQD	
156 157	1 0 7-3 2 1 0 7-4	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented Rx Disable implemented Rx Polarity Flip implemented Reserved	nted	Description 1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 1b=Rx Disable implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 1b=Rx Polarity Flip implemented	RO RQD RQD RQD RQD RQD RQD	
156 157	1 0 7-3 2 1 0 7-4 3	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl	nted	Description 1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 1b=Rx Disable implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Rx Polarity Flip implemented 0b=Rx Polarity Flip implemented 0b=Rx Polarity Flip implemented 0b=Rx Polarity Flip implemented 0b=Tx Adaptive Input Eq Fail flag not implemented	RO RQD RQD RQD RQD RQD RQD RO RQD RO	
156 157	1 0 7-3 2 1 0 7-4 3	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl implemented	nted	1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 0b=Rx Squelch Disable not implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip not implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip not implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Tx Adaptive Input Eq Fail flag not implemented 1b=Tx Adaptive Input Eq Fail flag implemented	RO RO RQD RO RQD RQD RO RQD RO RQD RO RQD	
156 157	1 0 7-3 2 1 0 7-4 3 2	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl implemented Tx CDR LOL flag implemented	nted ag nted	1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip not implemented 0b=Rx Polarity Flip implemented 0b=Rx Polarity Flip not implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Tx Adaptive Input Eq Fail flag not implemented 0b=Tx CDR Loss of Lock flag not implemented	RO RQD RQD RQD RQD RQD RO RQD RO RQD	
156 157	1 0 7-3 2 1 0 7-4 3 2	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl implemented Tx CDR LOL flag implemented	nted ag ited	1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable not implemented 0b=Rx Squelch Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Rx Polarity Flip implemented 0b=Tx Adaptive Input Eq Fail flag not implemented 0b=Tx CDR Loss of Lock flag not implemented 1b=Tx CDR Loss of Lock flag implemented	RO RQD RQD RQD RQD RQD RQ RQD RQ RQD	
156 157	1 0 7-3 2 1 0 7-4 3 2 1	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl implemented Tx CDR LOL flag implemented	nted ag nted	1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable not implemented 0b=Rx Squelch Disable not implemented 0b=Rx Squelch Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Rx Polarity Flip implemented 0b=Rx Polarity Flip implemented 0b=Rx Polarity Flip implemented 0b=Rx Polarity Flip implemented 0b=Tx Adaptive Input Eq Fail flag not implemented 0b=Tx CDR Loss of Lock flag not implemented 1b=Tx CDR Loss of Lock flag implemented 0b=Tx Loss of Signal flag not implemented	RO RQD RQD RQD RQD RQD RQD RQD	
156 157	1 0 7-3 2 1 0 7-4 3 2 1 2 1	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl implemented Tx CDR LOL flag implemented	nted ag nted	Description 1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable not implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Rx Polarity Flip implemented 0b=Tx Adaptive Input Eq Fail flag not implemented 1b=Tx CDR Loss of Lock flag not implemented 0b=Tx Loss of Signal flag not implemented 1b=Tx Loss of Signal flag implemented 1b=Tx Loss of Signal flag implemented 1b=Tx Loss of Signal flag implemented	RO RQD RQD RQD RQD RQD RQD RQD	
156 157	1 0 7-3 2 1 0 7-4 3 2 1 0	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl implemented Tx CDR LOL flag implemented Tx LOS flag implemented Tx Fault flag implemented	ag	Description 1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable not implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Rx Polarity Flip implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Tx Adaptive Input Eq Fail flag not implemented 1b=Tx CDR Loss of Lock flag not implemented 0b=Tx Loss of Signal flag not implemented 0b=Tx Loss of Signal flag not implemented 1b=Tx Loss of Signal flag implemented 0b=Tx Fault flag not implemented 1b=Tx Fault flag not implemented	RO RQD RQD RQD RQD RQD RQD RQD	
156 157 158	1 0 7-3 2 1 0 7-4 3 2 1 0 7-3	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl implemented Tx CDR LOL flag implemented Tx LOS flag implemented Reserved Reserved	nted ag nted	Description 1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 0b=Rx Polarity Flip not implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip not implemented 0b=Tx Adaptive Input Eq Fail flag not implemented 1b=Tx CDR Loss of Lock flag not implemented 0b=Tx CDR Loss of Lock flag implemented 0b=Tx Loss of Signal flag not implemented 1b=Tx Loss of Signal flag implemented 0b=Tx Fault flag not implemented 1b=Tx Fault flag implemented	RO RO RQD RO RQD RO RQD RO RQD RO RO RO RO RO	
156 157 158	1 0 7-3 2 1 0 7-4 3 2 1 0 7-3 2	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl implemented Tx CDR LOL flag implemented Tx Fault flag implemented Reserved	nted ag nted	Description 1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Polarity Flip not implemented 0b=Tx Polarity Flip implemented 0b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 0b=Rx Squelch Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 0b=Rx Polarity Flip not implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Tx Adaptive Input Eq Fail flag not implemented 1b=Tx CDR Loss of Lock flag not implemented 0b=Tx Loss of Signal flag implemented 0b=Tx Loss of Signal flag implemented 0b=Tx Fault flag not implemented 0b=Tx Fault flag implemented 0b=Tx Fault flag implemented	RO RQD RQD RQD RQD RQD RQD RQD RQD RQD RQD	
156 157 158	1 0 7-3 2 1 0 7-4 3 2 1 0 7-3 2	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl implemented Tx CDR LOL flag implemented Tx LOS flag implemented Reserved Reserved Reserved Rx LOL flag implemented	nted ag nted	1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable not implemented 0b=Rx Polarity Flip not implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Rx Polarity Flip implemented 0b=Rx Polarity Flip implemented 0b=Rx CDR Loss of Lock flag not implemented 1b=Tx CDR Loss of Signal flag implemented 0b=Tx Fault flag implemented 0b=Tx Fault flag implemented 1b=Tx Fault flag implemented 0b=Tx Fault flag implemented 0b=Tx Fault flag implemented 0b=Tx CDR Loss of Lock flag implemented 1b=Tx CDR Loss of Lock flag implemented 1b=Rx CDR Loss of Lock flag implemented	RO RQD RQD RQD RQD RQD RQD RQD RQD RQD RQD	
156 157 158	1 0 7-3 2 1 0 7-4 3 2 1 0 7-4 3 2 1 0 7-3 2 1	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl implemented Tx CDR LOL flag implemented Tx Fault flag implemented Reserved Rx LOL flag implemented Rx LOL flag implemented	nted ag nted	Description 1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable not implemented 0b=Rx Dolarity Flip not implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Rx CDR Loss of Lock flag not implemented 1b=Tx CDR Loss of Lock flag implemented 0b=Tx Fault flag not implemented 1b=Tx Fault flag not implemented 0b=Tx Fault flag not implemented 1b=Tx Fault flag implemented 0b=Tx CDR Loss of Lock flag not implemented 1b=Rx CDR Loss of Lock flag implemented 0b=Rx CDR Loss of Lock flag implemented 0b=Rx Loss of Signal flag not implemented 0b=Rx Loss of Signal flag not implemented	RO RQD RQD RQD RQD RQD RQD RQD RQD RQD RO RQD RO RQD RO RQD	
156 157 158	1 0 7-3 2 1 0 7-4 3 2 1 0 7-3 2 1	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl implemented Tx CDR LOL flag implemented Tx LOS flag implemented Reserved Reserved Rx LOL flag implemented Rx LOL flag implemented	nted ag nted	Description 1b=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable not implemented 0b=Rx Dolarity Flip not implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Rx Polarity Flip implemented 0b=Rx Polarity Flip not implemented 1b=Rx Dolarity Flip implemented 0b=Rx CDR Loss of Lock flag not implemented 1b=Tx CDR Loss of Lock flag implemented 0b=Tx Loss of Signal flag implemented 0b=Tx Fault flag not implemented 1b=Tx Fault flag implemented 0b=Tx CDR Loss of Lock flag not implemented 1b=Tx CDR Loss of Lock flag implemented 0b=Rx CDR Loss of Lock flag implemented 0b=Rx Loss of Signal flag not implemented 1b=Rx Loss of Signal flag not implemented 1b=Rx Loss of Signal flag implemented	RO RQD RQD RQD RQD RQD RQD RQD RQD RQD RQD	
156 157 158	1 0 7-3 2 1 0 7-4 3 2 1 0 7-3 2 1 0 7-3 2 1	Tx Disable implemented Tx Polarity Flip implemented Reserved Rx Squelch Disable implemented Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl implemented Tx CDR LOL flag implemented Tx LOS flag implemented Reserved Rx LOL flag implemented Rx LOS flag implemented Rx LOS flag implemented Rx LOS flag implemented	nted ag nted	Ib=Tx Squelch Disable implemented 0b=Tx Disable not implemented 1b=Tx Disable implemented 0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable not implemented 0b=Rx Squelch Disable implemented 0b=Rx Disable not implemented 0b=Rx Disable not implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Rx Polarity Flip implemented 0b=Rx Polarity Flip implemented 0b=Rx Polarity Flip implemented 0b=Rx Polarity Flip implemented 0b=Tx Adaptive Input Eq Fail flag not implemented 1b=Tx CDR Loss of Lock flag not implemented 1b=Tx CDR Loss of Lock flag implemented 0b=Tx Fault flag not implemented 1b=Tx Fault flag implemented 0b=Tx Fault flag implemented 0b=Tx CDR Loss of Lock flag not implemented 1b=Rx CDR Loss of Signal flag not implemented 0b=Rx Loss of Signal flag not implemented 0b=Rx Loss of Signal flag not implemented <t< td=""><td>RO RQD RQD RQD RQD RQD RQD RQD RQD RQD RQD</td></t<>	RO RQD RQD RQD RQD RQD RQD RQD RQD RQD RQD	

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Byte	Bit	Name	Description	Туре
159	7-6	Reserved	•	RO
				RQD
				-
	5	Custom monitor implemented	0b=Custom monitor not implemented	RO
			1b=Custom monitor implemented	RQD
	4	Aux 3 monitor implemented	0b=Aux 3 monitor not implemented	
			1b=Aux 3 monitor implemented	
	3	Aux 2 monitor implemented	0b=Aux 2 monitor not implemented	
			1b=Aux 2 monitor implemented	
	2	Aux 1 monitor implemented	0b=Aux 1 monitor not implemented	
			1b=Aux 1 monitor implemented	
	1	Internal 3.3 Volts monitor	0b=Internal 3.3 V monitor not implemented	
		implemented	1b=Internal 3.3 V monitor implemented	
	0	Temperature monitor	0b=Temperature monitor not implemented	
		implemented	1b=Temperature monitor implemented	
160	7-5	Reserved		RO
	4-3	Tx Bias current measurement	Multiplier for 2uA Bias current increment used in Tx Bias	RQD
		and threshold multiplier	current monitor and threshold registers (see Table 8-42	
			and Table 8-62)	
			00b=multiply x1	
			01b=multiply x2	
			10b=multiply x4	
			11b=reserved	-
	2	Rx Optical Input Power monitor	0b=Rx Optical Input Power monitor not implemented	
		implemented	1b=Rx Optical Input Power monitor implemented	-
	1	Tx Output Optical Power monitor	0b=Tx Output Optical Power monitor not implemented	
		Implemented	1b=1x Output Optical Power monitor implemented	-
	0	Ix Bias monitor implemented	Ob=1x Bias monitor not implemented	
			ID= IX Bias monitor implemented	
161	7	Reserved		RO
	6.5	T. T. L. F. OL. (D. 111. (C.		RQD
	0-D	TX Input Eq Store/Recall buller	00D=1X Input Eq Store/Recall hot implemented	RU
		count	10b=Tx Input Eq Store/Recall buffer count=1	RQD
			10D=1X Input Eq Store/Recail burler count=2	
	4	Ty Input Ed Franza implemented	Ob-Ty Input Ed Freeze net implemented	-
	4	TX Input Eq Freeze implemented	1b=Tx Input Eq Freeze implemented	
	3	Adaptive Tx Input Eq.	0b=Adaptive Tx Input Eq not implemented	-
	5	implemented	1b=Adaptive Tx Input Eq inclimplemented	
	2	Tx Input Eq fixed manual control	Ob=Tx Input Eq Fixed Manual control not implemented	-
	2	implemented	1b=Tx Input Eq Fixed Manual control implemented	
	1	Tx CDR Bypass control	0b=Tx CDR Bypass control not implemented (if CDR is	
	-	implemented	implemented, it will be enabled)	
			1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented	1
		• • • • • • • • •	1b=Tx CDR implemented	
162	7-6	Reserved		RO
				RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Page 10h	RO
	4-3	Rx Output Eq control	00b=Rx Output Eq control not implemented	RQD
		implemented	01b=Rx Output Eq Pre-cursor control implemented	
			10b=Rx Output Eq Post-cursor control implemented	
			11b=Rx Output Eq Pre- and Post-cursor control	
			implemented	
	2	Rx Output Amplitude control	0b=Rx Output Amplitude control not implemented	
		implemented	1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control	0b=Rx CDR Bypass control not implemented (if CDR is	
		implemented	implemented, it will be enabled)	
			1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented	
			1b=Rx CDR implemented	



4.7 Load/Save MSA

This tab allows the user to Load or Save his custom MSA configuration.

Data is displayed in a grid showing: register address, hex value, Decimal Values, ASCII value, MSA description.

Also the buttons available in this tab are summarized below:

- **Refresh Page**: Read MSA Registers, and refresh values.
- Write MSA to HW: Write the current MSA configuration to the module.
- Save MSA to file: Save the current MSA memory to a file using Comma separated values (CSV) format.
- Load MSA from file: Load MSA values from file and map it to MSA memory.
- Checksum for pages 00, 01 and 02

	Refresh Page	W	rite MSA to HW	- Lo	oad MSA from file	Save MSA to file	
	Address	Data(Hex)	Data(Dec.)	Data(Ascii)	MSA Description	<u> </u>	
•	LowMem 0(00h)	0	0	0	Identifier		
	LowMem 1(01h)	0	0	0	Revision Compliance		Checksum (Page00 128-221)
	LowMem 2(02h)	0	0	0	CLEI code present		Stored
	LowMem 3(03h)	0	0	0	Module State		Calculated
	LowMem 4(04h)	0	0	0	Bank 0 flag summary		
	LowMem 5(05h)	0	0	0	Bank 1 flag summary		Checksum (Page01 130-254)
	LowMem 6(06h)	0	0	0	Bank 2 flag summary		Stored
	LowMem 7(07h)	0	0	0	Bank 3 flag summary		Calculated
	LowMem 8(08h)	0	0	0	Data Path/Module firm	ware fault and Module S	
	LowMem 9(09h)	0	0	0	Latched VCC3.3/Temp	Alarm and Warning	Checksum (Page02 128-254)
	LowMem 10(0Ah)	0	0	0	Latched AUX1/2 Alarm	and Warning	Stored
	LowMem 11(0Bh)	0	0	0	Latched Vendor Define	ed/AUX3 Alarm and Warn	
	LowMem 12(0Ch)	0	0	0	Reserved		Calculated
	LowMem 13(0Dh)	0	0	0	Custom		
	LowMem 14(0Eh)	0	0	0	Internally measured Te	emperature 1 MSB	
	LowMem 15(0Fh)	0	0	0	Internally measured Te	emperature 1 LSB	
	LowMem 16(10h)	0	0	0	Internally measured Su	ipply 3.3v MSB	
	LowMem 17(11h)	0	0	0	Internally measured Su	ipply 3.3v LSB	
	LowMem 18(12h)	0	0	0	Internally measured AU	JX1 MSB	
	LowMem 19(13h)	0	0	0	Internally measured AU	JX1 LSB	
	LowMem 20(14h)	0	0	0	Internally measured AU	JX2 MSB	

Figure 13: Load/Save MSA Tab

4.8 Load/Save Page 10/11h

This tab allows the user to Load or Save configuration for Page10h and Page11h. Data is displayed in a grid showing: register address, hex value, Decimal Values, ASCII value and MSA description. Buttons in this tab are described below:

- **Refresh Page**: Read Registers, and refresh values.
- Write MSA to HW: Write the current MSA configuration to the module.
- Save MSA to file: saves the current MSA memory to a file using Comma separated values (CSV) format.
- Load MSA from file: Loads MSA values from file and map it to MSA memory.



Refresh Page	Write M	SA to HW	Load MSA f	rom file Save MSA to file
Address	Data(Hex)	Data(Dec.)	Data(Ascii)	MSA Description
Page16(10h) 253(FDh)	0	0	0	Custom
Page16(10h) 254(FEh)	0	0	0	Custom
Page16(10h) 255(FFh)	0	0	0	Custom
Page17(11h) 128(80h)	0	0	0	Datapath State Encoding
Page17(11h) 129(81h)	0	0	0	Datapath State Encoding
Page17(11h) 130(82h)	0	0	0	Datapath State Encoding
Page17(11h) 131(83h)	0	0	0	Datapath State Encoding
Page17(11h) 132(84h)	0	0	0	Reserved
Page17(11h) 133(85h)	0	0	0	Reserved
Page17(11h) 134(86h)	0	0	0	Latched Data Path State Changed flag
Page17(11h) 135(87h)	0	0	0	Latched Tx Fault flag
Page17(11h) 136(88h)	0	0	0	Latched Tx LOS flag
Page17(11h) 137(89h)	0	0	0	Latched Tx CDR LOL flag
Page17(11h) 138(8Ah)	0	0	0	Latched Tx Adaptive Input Eq. Fault
Page17(11h) 139(8Bh)	0	0	0	Tx output power High Alarm
Page17(11h) 140(8Ch)	0	0	0	Tx output power Low Alarm
Page17(11h) 141(8Dh)	0	0	0	Tx output power High Warning
Page17(11h) 142(8Eh)	0	0	0	Tx output power Low Warning
Page17(11h) 143(8Fh)	0	0	0	Tx Bias High Alarm

Load/Save Page 10/1

Figure 14: Load/Save Page 10/11h Tab

4.9 I2C R/W

This tab gives access to MSA registers.

- 1. Select the page in the **Memory Location**.
- 2. **Single Byte** window: to read/write one byte from the memory.
 - a. Address: The address to read/write from.
 - b. Memory Content: The data value read from or written to the selected address.

3. **Multi-bytes** window: to read multiple bytes between selected Starting Address and an End Address.

Refresh Page							
		Multiple Byte	es				
Page 01(Optional)	Upper Page 02(Option	nal) Starting A (Decimal)	ddress	End Address (Decimal)		Read	Save
Set		Address	Hex	Binary	ASCII		
ent Memory Content (Binary)	ASCII	_					
Write							
te	Set tent Memory Content (Binary) Write	Set Set tent Memory Content (Binary) ASCII Write	Set (Decimal) Address Write	Set	Set (Decimal) (Decimal) (Decimal) (Address Hex Binary Write	Set (Decimal) (D	Set (Decimal) (Decimal) (Decimal) Read Address Hex Binary ASCII (Binary) Write

Figure 15: I2C R/W Tab



4.10 QDD MXP

This tab is used only with ML4062-MCB-MXP.

The following tab allows the user to modify the DC Level within a range between 3.0 and 3.6, and to insert noise to the VCC by adding noise frequency between 0 and 12500000 Hz and control noise amplitude ranging from 0 to 120mV.

Two buttons are available under Noise Insertion Window:

- 1. Apply: this must be pressed so the noise frequency and amplitude take effect
- 2. Reset: this will set noise frequency and amplitude back to 0

									QDD MXP	
Th	is tab is on	v availa	able for MI 40)62-MCB-N	XP					
		iy urun		702 meb m						
VC	C				Noi	se Insertion				
					Ne	oise Frequency:	0 Hz			
			_							
1	DC Level:		U	3.3 V	No	oise Amplitude:	U	0	mV	
							Apply	Reset		
								- Contract		
N.B:	Press Enter each t	time you wri	te a value in a textbo	ox.						

Figure 16: QDD MXP Tab

4.11 I2C R/W Advanced

This tab gives access to MSA registers without specifying the Slave address.

- 1. Select Page Number under Memory Location window.
- 2. Under **Single Byte** window.
 - Write the corresponding Slave Address
 - o Write the Address to read from or write to
 - Data to be written to or Read from the selected address is under Memory Content field
- 3. Under Multi-Byte Read window.
 - o Write the corresponding Slave Address
 - \circ $\;$ Select the Starting Address and the End Address to Read from



										I2C R/W Advanced	
Men	nory Location			Single Byte							
Pa	ge Number(Decimal	.)		Enter ASCII or	Hex or Binary						
0	0		Set	Slave Address	(Hex) Address(decimal) Me	emory Content(Hex)	Memory Conte	nt(binary)	ASCII	
				<u> </u>							
						Read	Write				
				Multi-Byte Rea	ad						
				Slave Address(Hex) Starting Ad (Decimal)	ldress End Ad (Decim	dress nal)				
							Read				
				Address	Hex	Binary A	SCII				

Figure 17: I2C R/W Advanced Tab

4.12 Command Data Block (CDB) Message Communication

The Common Data Block (CDB) is a message communication protocol between the Host and a Module that allows the user to check and apply various settings on the interconnect, including updating the firmware. CDB is a Two Wire serial Interface (TWI) protocol based on the i2c for CMIS 4.0 and 5.0 between a Master (Initiator in 5.0) and Slave (Target in 5.0).

The host sends a CDB Command (CMD) message which is identified by a CMD ID and the module responds with a CDB Reply (REPLY) message without changing the CMD ID.

On the ML4062 Module Compliance Board (MCB), the CDB enables the issuing of commands from the MCB to the interconnect. The ML4062 MCB includes all CDB commands mentioned in CMIS 4.0 and CMIS 5.0.

 Monitor
 CDB
 Interrupt Masks
 Controls
 Low Speed Signals
 Identification
 Options Available
 Load/Save MSA

 Unlock CDB Feature
 CDB Commands
 CDB Feature and Capabilities Commands
 CDB Firmware Download Commands
 CDB Performance/Data Monitoring Commands

 CDB License
 Snowse
 C:Utsers/User/Desktop
 Uicense.bt
 Validate
 Validate</

Unlock CDB feature by loading the purchased License File:

Figure 21: CDB License Validation



4.12.1 CDB Commands

- CMD 0000h Query Status
- CMD 0001h Enter Password
- CMD 0002h Change Password
- CMD 0003h Enable/Disable Password Protection
- CMD 0004h General Abort
- CMD 0380h Loopbacks

B Module Commands	CDR	Detailed Map Registers				
Delay MSB (Dec) Delay LSB (Dec)						
0 0 Ouery Status		Name CDP. Status	Page (Hex)	Address (Hex)	Value (Hex)	
	r i	CDB Complete Flag	00	23	01	
		Length of status	9F	88	03	
Password Entry/ Change (Dec)		Unlock level and privileges	9F	89	00	
0 0 16 17		Firmware download allowed	9F	8A	00	
Set Password Change Password	•					
General Abort	Suc	cess				
mmand Progress						

Figure 22: CDB Commands

The CDB GUI includes detailed map registers that show what is returned by each command.

Here, for example, the query status command is being sent. A progress bar indicates the progress of the running CDB command. The GUI clearly indicates that the command was sent successfully (CDB status=1), that it asserts the CDB flag, and that it returns three bytes of data as shown with the corresponding value and description. The User can export this data (to an excel sheet) using the export button.

4.12.2 CDB Feature and Capabilities Commands

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- **CMD 0040h Module Features**: Identifies which commands are supported, from CMD 0 to CMD 00FF along with the maximum CDB command execution time.
- CMD 0042h Performance Monitoring: Identifies which commands are supported from 0200h to 02FFh.
- CMD 0043h Bert and diagnostics: Identifies CMD 0300h to 03FFh.
- CMD 0041h Read FW Features: Identifies many parameters supported the firmware features including firmware download transfer type, if copy/abort/full image readback commands are supported, start command payload size, erased byte, the firmware update features, if read/write firmware is supported, the firmware can be upgraded, etc. Use this feature to determine whether a device supports LPL or EPL firmware.

Module Features	Performance	• Monitoring	Bert And Dia	gnostic	Name	Page (Hex)	Address (Hex)	Value (Hex)	Description
			-		CDB Status	00	25	01	Success
ommand support	0 3	4 7	8 B	C F	CDB Complete Flag	00	80	00	CDB Complete Flag Assertion
CMDs 0000h - 000Fh				0000	Reserved	9F	89	00	Reserved
MDs 0010h - 001Fh	0000			0000	CMDs 0000h-0007h support	9F	8A	07	Each bit represent a mask. If bit is
CMDs 0020h - 002Fh	0000			0000	CMDs 0008h-000Fh support	9F	8B	00	Each bit represent a mask. If bit is
CMDs 0030h - 003Fh	0000			0000	CMDs 0010h-0017h support	9F	8C	00	Each bit represent a mask. If bit is
CMDs 0040h - 004Fh		0000		0000	CMDs 0018h-001Fh support	9F	8D	00	Each bit represent a mask. If bit is
CMDs 0050h - 005Fh	0000			0000	CMDs 0020h-0027h support	9F	8E	00	Each bit represent a mask. If bit is
CMD: 0060b - 006Fb	0000			00000	CMDs 0028h-002Fh support	9F	8F	00	Each bit represent a mask. If bit is
CMDs 0030h - 003Fh	0000			00000	CMDs 0030h-0037h support	9F	90	00	Each bit represent a mask. If bit is
CMDs 0070H - 007Fh	0000			0000	1	14		000	Ladron represent a master i pre p
CMDs 0080h - 008Fh	0000			0000					Event
CMDs 0090h - 009Fh	0000			0000					Export
CMDs 00A0h - 00AFh				0000					
CMDs 00B0h - 00BFh				0000	Command Progress				
CMDs 00C0h - 00CFh	0000			0000					
CMDs 00D0h - 00DFh	0000			0000	Success				
CMDs 00E0h - 00EFh				0000					
				0000					

Figure 23: CDB Feature and Capabilities Commands

The green buttons indicate which commands are supported. In this case, the module feature command is returning the corresponding data in the detailed map register and indicates that CMDs 0,1,2,40,41,42,43 are supported (other modules might support other commands).

4.12.3 CDB Firmware Download Commands

- CMD 0101h, 0103h, 0107h Program LPL: Loads the firmware binary file for Local Payload (LPL). Allows for updating interconnect firmware.
- CMD 0101h, 0104h, 0107h Program EPL: Loads the firmware binary file for Extended Payload (EPL). EPL support varies depending on the interconnect. Allows for updating interconnect firmware.
- CMD 0101h, 0105h, 0107h Read Image LPL: Read the latest upgraded firmware image using LPL

 CMD 0101h, 0106h, 0107h Read Image EPL: Read the latest upgraded firmware image using EPL.

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- Export Image: Exports an image of the firmware after the read is completed as a .bin file, which in turn can be loaded into and read by other interconnects.
- CMD 0102h Abort FW download: Stops the firmware from being installed onto the interconnect.
- **CMD 0109h Run image**: After the new LPL or EPL Firmware is loaded, this command switches to the latest firmware image. Does not replace the existing firmware image on the interconnect.
- CMD 010Ah Commit image: Replaces the firmware image on the interconnect with the new loaded firmware image. Prior to this command being executed, the old firmware will still be executed on startup. Always ensure the new image is running perfectly (by running it on the interconnect using the previous commands) before using this command.
- CMD 0108h Copy image A to B/B to A: In the event of two images being present on the same interconnect and both images are written to flash, this command makes ensures that both images are identical, with the copied image being specified in the commands as either image A to image B, or image B to image A.
- **CMD 0100h Get FW Info**: Loads the information about the latest firmware on the interconnect, for both image A and image B.

DB Firmware Download Co	mmands		Ge	t Firmware Info				
oad corresponding binary	y file			Get FW Info				
C:\Users\User\Desktop \400GSR8_034ATN_SOFT_\	/130T01_CDB.bin	Browse						
			CD	B Detailed Map Registers				
				Name	Page (Hex)	Address (Hex)	Value (Hex)	Description
Download new firmware i	image		•	CDB Status	00	25	01	Success
Descent I DI Desc	THE FOI			CDB Complete Flag	00	08	00	CDB Complete Flag Assertion
Program LPL Prog	ram CPL			Firmware Status Flags	9F	88	03	Bitmask to indicate FW Status.00h: Fa
B				Information block	9F	89	01	Bit 0: Firmware image A is present in
Read latest downloaded	firmware image			Image A Major	9F	8A	01	Image A Major revision
Read Image LPL Read I	mage EPL	Export Image		Image A Minor	9F	8B	03	Image A Minor revision
				Image A Build	9F	8C	00	Image A Build number
Abort firmusro download				Image A Build	9F	8D	01	Image A Build number
Abort minimare dominoad				Image A Extra String	9F	8E	01	Image A Extra String
Abort Firmware				Image A Extra String	9F	8F	02	Image A Extra String
				Image A Extra String	9F	90	02	Image A Extra String
Run downloaded firmware	e image			Image A Extra String	9F	91	00	Image A Extra String
Delay MSB (Dec) Delay L	SB (Dec) Reset							
0 0		*						Export
Pup Image	Traffic af	fecting Reset to Inactive Image						
Null Illinge	Attempt	Hitless Reset to Inactive Image	Co	mmand Progress				
Switch to the new firmura	Traffic of	festing Paret to Pupping Image	_					
Switch to the new firmwa	are mage traffic at	recting Reset to Running Image	Sur	Cass				
Commit Image	Attempt	Hitless Reset to Running Image	Suc					

Figure 24: CDB Firmware Download Commands

4.12.4 CDB Performance/Data Monitoring Commands

CMD 0200h PM Controls: Extract Performance Monitoring data records such as minimum/average/maximum values. "No Operation" reads the most recent values, while "Clear All" clears the extracted values for all lanes in the interconnect.



- **CMD 0280h Data Monitoring and Recording Controls**: "Refresh" loads the most recent attributes. "Clear All" clears all values for all parameters for all lanes at the same time.
- CMD 0281h Data monitoring and recording advertisement

multiLane

- **CMD 0290h Temperature Histogram**: Displays the temperature intervals of the interconnect and how long it stayed at each temperature interval.
- CMD 0210h, 0211h Get Module PM LPL/EPL: Choose parameters of the module's performance monitoring records, and replace the current values of the minimum, average, and maximum values. "Refresh" replaces the old values, while "Clear and Read" reads and resets the old values.
- CMD 0212h, 0213h Get PM Host Side LPL/EPL: Choose parameters of the host's performance monitoring records, and replace the current values of the minimum, average, and maximum values. "Refresh" replaces the old values, while "Clear and Read" reads and resets the old values.
- CMD 0214h, 0214h Get PM Media Side LPL/EPL: Choose parameters the performance monitoring records of specific lanes, and replace the current values of the minimum, average, and maximum values. "Refresh" replaces the old values, while "Clear and Read" reads and resets the old values.
- CMD 0216h, 0217h Get Data Path PM LPL/EPL: Choose the data path for specific lanes and replace the current values of the minimum, average, and maximum values. "Refresh" replaces the old values, while "Clear and Read" reads and resets the old values.



Figure 25: CDB Performance/Data monitoring Commands



Software Revision

V2.2.1: latest Software Revision, which this document is based on.





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